PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-168308
(43)Date of publication of application : 22.06.2001

(51)Int.Cl. H01L 27/12
H01L 21/306
H01L 29/786

(21)Application number : 2000-288734
(22)Date of filing : 22.09.2000

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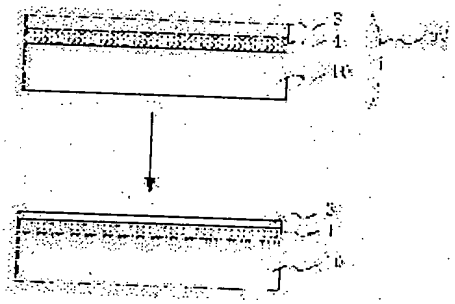
(30)Priority
Priority number : 11278937 Priority date : 30.09.1999 Priority country : JP

(54) METHOD OF MANUFACTURING SILICON THIN FILM, FORMING METHOD OF SOI SUBSTRATE, AND SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the thickness of a silicon thin film to a prescribed value without deteriorating it in quality and avoiding it that the oxidation of crystal defects generated when a usual sacrificial oxidation is carried out is accelerated, the surface is roughened by the influence of a foreign object, and an oxide film is deteriorated in withstand voltage due to the fact that the surface gets rough.
SOLUTION: A SOI wafer provided with a silicon thin film which deposits oxygen little is prepared through an SIMOX method or a lamination method, the SOI wafer is cleaned with an alkaline solution such as SCI or TMAH, and a silicon ultra-thin film SOI is manufactured by the etching action of the alkaline solution.



LEGAL STATUS
[Date of request for examination]
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the silicon thin film characterized by including the process which decreases the thickness of this silicon thin film until it becomes thickness 100nm or less by carrying out wet washing of the silicon thin film prepared on said insulating front face in the manufacture approach of the silicon thin film for manufacturing the silicon thin film prepared on the insulating front face.
[Claim 2] The 1st thickness of said silicon thin film before [said] carrying out wet washing is the manufacture approach of the silicon thin film according to claim 1 characterized by performing this wet washing until it is larger than 100nm and becomes the 2nd thickness thinner than this 1st thickness after heat-treating this silicon thin film that has this 1st thickness in the reducing atmosphere containing hydrogen.
[Claim 3] The manufacture approach of a silicon thin film according to claim 2 that said 2nd thickness is 50nm or less.
[Claim 4] Said silicon thin film is the manufacture approach of the silicon thin film according to claim 1 obtained from the epitaxial growth film.
[Claim 5] Said silicon thin film is the manufacture approach of the silicon thin film according to claim 1 obtained from the silicon by which hydrogen annealing was carried out.
[Claim 6] Said silicon thin film is the manufacture approach of the silicon thin film according to claim 1 obtained from FZ silicon wafer.
[Claim 7] Said wet washing is the manufacture approach of the silicon thin film according to claim 1 which is washing which used SC1 penetrant remover or the organic alkali solution.
[Claim 8] The etch rate by said wet washing is the manufacture approach of a silicon thin film according to claim 1 when it is the following by 10nm/above by 0.1nm/.
[Claim 9] Said silicon thin film is the manufacture approach of the silicon thin film according to claim 1 with which wet washing processing is presented, without oxidizing thermally.
[Claim 10] Said silicon thin film is the manufacture approach of the silicon thin film according to claim 1 which consists of silicon film with oxygen content lower than CZ wafer.
[Claim 11] Said wet washing is the manufacture approach of the silicon thin film according to claim 1 which is washing using the penetrant remover containing ammonia and a hydrogen peroxide.
[Claim 12] The manufacture approach of the SOI substrate characterized by including the process which carries out wet washing of this base after the process which prepares the base which has the silicon thin film of the 1st larger thickness than 100nm on an insulating front face, the heat treatment process which heat-treats this base in the reducing atmosphere containing hydrogen, and this heat treatment process, and makes this silicon thin film the thickness of the 2nd thickness thinner than this 1st thickness.
[Claim 13] The production approach of the SOI substrate according to claim 12 formed including the process which separates this compound member by the porous layer after said base sticks the 1st substrate and 2nd substrate which have a silicon thin film through an insulating layer and forms a compound member on a porous layer.
[Claim 14] The production approach of the SOI substrate according to claim 12 formed including

the process which separates this compound member in this ion-implantation layer after said base sticks the 1st substrate and 2nd substrate which have a silicon thin film through an insulating layer and forms a compound member on an ion-implantation layer.
[Claim 15] Said 1st substrate is the production approach of the SOI substrate according to claim 12 formed in a silicon wafer including the process which pours a hydrogen ion into a predetermined field.
[Claim 16] Said base is the manufacture approach of the SOI substrate according to claim 12 currently formed including the process which pours oxygen ion into a silicon wafer.
[Claim 17] The production approach of a SOI substrate according to claim 12 that said 2nd thickness is 50nm or less.
[Claim 18] The silicon thin film manufactured by the manufacture approach of a silicon thin film according to claim 1 to 11.
[Claim 19] The SOI substrate produced by the approach according to claim 12 to 17.
[Claim 20] The manufacture approach of the semiconductor device characterized by forming the active region of a transistor in said silicon thin film according to claim 12.
[Claim 21] The semiconductor device characterized by forming the active region of a transistor in said silicon thin film according to claim 12.
[Claim 22] Said transistor is a semiconductor device according to claim 19 which is the thin film MOS transistor of a partial depletion mold.
[Claim 23] Said transistor is a semiconductor device according to claim 20 which is the thin film MOS transistor of a perfect depletion mold.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the approach of controlling the thickness of the silicon thin film used for a SOI wafer etc., and the manufacture approach of a silicon thin film about the manufacture approach of a silicon thin film. Silicon thickness is decreased by wet washing and, more specifically, it belongs to the technical field which obtains the thickness of arbitration.
[0002]
[Description of the Prior Art] as the manufacture approach of a SOI wafer -- SIMOX (Separetion by IMplanteion of OXygen) -- law, a lamination method, etc. are learned.
[0003] The SIMOX method is a technique which forms a silicon oxide layer in the location which drove in oxygen ion from the front face of a silicon substrate, and was embedded by subsequent elevated-temperature annealing. The dose of impregnation energy ** of the oxygen ion at this time cannot be set to arbitration, but is set to about certain conditions. Therefore, the SOI wafer which can come to hand can change neither silicon thickness nor thickness of an embedding oxide film into arbitration easily.
[0004] There are some classes of lamination methods. The approach currently called "the lamination polish SOI" etc. is mentioned first.
[0005] It is the approach of preparing two wafers with which at least one side oxidized, grinding these with grinding from one side at a room temperature after annealing, lamination and, and leaving the silicon thickness of arbitration on a silicon oxide layer. By this approach, the thickness of a silicon layer and the thickness of an embedding silicon oxide layer can be set as arbitration. However, in order to depend for thin film-ization of a silicon layer only on grinding and polish, the thin film of hundreds of nm uniform thickness is difficult to get by the limitation of the original thickness precision of a silicon wafer, and the precision of polish.
[0006] In order to compensate the above-mentioned fault, distribution of SOI thickness is measured in an instant, dry etching of the field and thinner is carried out few, and the technique which forms a super-thin film (100nm or less) in homogeneity is reported. [field / thicker] This technique was called PACE (Plasma Assisted Chemical Etching) and is divided into the unit which carries out field Uchida point (10000 or more points) measurement of the SOI thickness in an instant as mentioned above, and the unit which carries out plasma etching. To the unit of etching, it has the plasma generating part of a nozzle mold, and it can move now along a field in the upper part of a wafer side so that the nozzle can etch more thick fields according to the measurement result of the thickness of a SOI layer. The amount of etching is controlled for every field within a wafer side, and the absolute value of thickness and homogeneity can be controlled. However, in order that an etching damage may remain in the front face by which plasma etching was carried out, polish for finally removing a damage layer is performed in many cases. Thickness which became homogeneity with much trouble by this action may be ununiformity-ized again.
[0007] moreover, the front face of the silicon wafer which the oxide film attached as another lamination method as it was in a U.S. Pat. No. 5374567 number -- a hydrogen ion -- pouring in -

- the interior of a wafer -- a brittle layer -- forming -- heating of an another wafer and lamination after that, and after that -- or there are some which spray a fluid (gases, such as liquids, such as water, or nitrogen) on a lamination wafer side face, dissociate from a brittle layer, and acquire SOI structure.

[0008] Control of thickness is controllable by the thickness of the oxide film of the wafer prepared first, the impregnation energy of a hydrogen ion, etc. However, to the dry area on the separated front face of SOI, polish finishing is needed in many cases and, thereby, thickness will become an ununiformity.

[0009] Moreover, as another lamination method, there is an approach indicated by a U.S. Pat. No. 5371037 number (patent No. 2608351), JP,5-21338,A, or JP,7-302889,A. This approach is an approach of removing an another wafer and lamination, and an unnecessary part for the silicon single crystal film which grew epitaxially on the substrate which has porosity silicon through an oxide film, and obtaining a SOI layer. Control of the thickness in this approach is made by control of epitaxial thickness and oxide-film thickness etc.

[0010] Although it may be ruined at the process which carries out selective etching of the porosity silicon which remains on a SOI layer front face if the front face after a process is observed, it is carrying out hydrogen annealing of the SOI layer front face as indicated by JP,5-218053,A, and is made in a very smooth field. According to this approach, degradation of distribution of the thickness of a SOI layer does not take place.

[0011]

[Problem(s) to be Solved by the Invention] However, even if it is these lamination methods, it is not easy for thickness to form a super-thin film 100nm or less directly, for example.

[0012] In order to remove the etching damage layer of the plasma which remains in a front face in the case of the PACE method, it is necessary to make a thicker SOI layer a little in consideration of a part for the thickness. However, since the damage layer removal is performed by polish, the thickness distribution variation by polish occurs and homogeneity formation of a super-thin film becomes difficult. By the approach which needs polish of a SOI layer for the same reason, direct formation of a super-thin film becomes difficult altogether.

[0013] Moreover, when the above-mentioned hydrogen annealing is used for smoothing of the SOI film, a pinhole may occur. It exists in a lamination interface. In a measuring instrument, stress is applied to the minute field by the side of the lamination interface of a super-thin film that it cannot measure with such a minute (90nm or less) foreign matter and the surface irregularity of the wafer itself. Under existence of this stress, if hydrogen annealing treatment is performed, a pinhole may occur to a stress generating part. On the other hand, in the case of the design of semiconductor devices, such as a transistor, when the SOI thickness demanded is still thinner than the minimum thickness which can be supplied as a SOI wafer, or when the SOI wafer of different thickness with modification of a design is needed, a wafer supply side cannot fully respond. In such a case, once the manufacturer of a semiconductor device receives beforehand the SOI wafer with a SOI layer thicker than design thickness and oxidizes the front face thermally, he has to perform sacrifice oxidization of removing the part which oxidized by etching, and has to get the SOI layer of desired thickness.

[0014] However, if sacrifice oxidation is performed, the accelerating oxidation over the crystal defect which exists in the SOI film has done enough, and since oxidation is checked around the field where the foreign matter adhered, the surface dry area of the front face of a SOI layer will be caused as a result. This becomes the cause of degrading oxide-film pressure-proofing of a semiconductor device.

[0015]

[Means for Solving the Problem] The purpose of this invention is to offer the thickness control approach of a silicon thin film that the value of a request of the thickness can be decreased, the manufacture approach of a silicon thin film, and the manufacture approach of a SOI substrate, without degrading the quality of a silicon thin film.

[0016] In the manufacture approach of the silicon thin film for manufacturing the silicon thin film prepared on the insulating front face, by carrying out wet washing of the silicon thin film prepared on said insulating front face, this invention is characterized by including the process

which decreases the thickness of this silicon thin film until it becomes thickness 100nm or less. Moreover, the manufacture approach of the silicon thin film concerning this invention of the 1st thickness of said silicon thin film before [said] carrying out wet washing is larger than 100nm, and it is characterized by performing this wet washing after heat-treating this silicon thin film that has this 1st thickness in the reducing atmosphere containing hydrogen until it becomes the 2nd thickness thinner than this 1st thickness. For example, said 2nd thickness is 100nm or less or 50nm or less.

[0017] The creation approach of the SOI substrate concerning this invention is characterized by to include the process which carries out wet washing of this base after the process which prepares the base which has the silicon thin film of the 1st larger thickness than 100nm on an insulating front face, the heat treatment process which heat-treats this base in the reducing atmosphere containing hydrogen, and this heat treatment process, and makes this silicon thin film the thickness of the 2nd thickness thinner than this 1st thickness.

[0018] After said base sticks the 1st substrate and 2nd substrate which have a silicon thin film through an insulating layer and forms a compound member on a porous layer, After being formed including the process which separates this compound member by the porous layer, or sticking the 1st substrate and 2nd substrate which have a silicon thin film through an insulating layer and forming a compound member on an ion-implantation layer, it is formed including the process which separates this compound member in this ion-implantation layer.

[0019] According to this invention, degradation of the oxide-film pressure-proofing accompanying the surface dry area under accelerating oxidation of the crystal defect section produced when performing the conventional sacrifice oxidation, the effect of a foreign matter, etc., and a surface dry area etc. is avoidable. Moreover, a thermal oxidation process and the etching process of the thermal oxidation film can be skipped.

[0020]

[Embodiment of the Invention] In this invention, as first shown in drawing 1 , the SOI substrate 50 is prepared, and wet washing is carried out, without oxidizing thermally the silicon thin film (SOI layer) 3 on the insulating layer 4 of the SOI substrate. The thickness of a SOI layer is made to decrease by this wet washing, and desired thickness is obtained. In addition, 10 is bases, such as silicon.

[0021] If it considers as the SOI layer used for this invention, the SOI layer of the SOI wafer produced by the SIMOX method mentioned above and the lamination method is desirable. and the SOI layer formed using the silicon thin film formed of epitaxial growth or hydrogen annealing or FZ (floating zone) -- CZ (CHOKURARU skiing) with the common SOI layer produced using the silicon substrate formed of law -- since oxygen content is low, it is more desirable than the silicon wafer formed of law. Moreover, a MCZ wafer is also desirable. In this way, the obtained SOI layer does not have sludges, such as silicon oxide, into it, and serves as a homogeneous silicon thin film. As a substrate which directs a silicon thin film, an insulator layer is the substrate or insulator substrate of the semi-conductor formed in the front face, or ******.

[0022] It is because uniform oxidization and uniform etching in the part will be checked if matter other than silicon deposits in a silicon thin film.

[0023] CZ (CHOKURARU skiing) -- when the silicon wafer obtained in law is used as a SOI layer, a defect will occur in silicon by deposit of oxygen, or a surface dry area will arise. The oxygen that in CZ silicon wafer contained is returned by hydrogen, the concentration becomes low, and a deposit is suppressed. [many] Therefore, after forming a SOI layer as a SOI layer by which hydrogen annealing was carried out, without giving hydrogen annealing, hydrogen annealing may be given to the SOI layer and a SOI layer may be formed using the silicon wafer which carried out hydrogen annealing.

[0024] The thickness of the SOI layer before reducing thickness by this invention is larger than 100nm, and the thickness of the SOI layer finally obtained is the very thin film of 100nm or less.

[0025] As a penetrant remover used for this invention, SC1 penetrant remover used by the so-called RCA washing is suitable. SC1 penetrant remover is NH4OH and H2O2. It consists of mixed liquor of H2O. 1:5:5, 1:10:10, 0.05:1:5, 0.05:1:10, etc. may have standard aqueous ammonia, hydrogen peroxide solution, and various water at a capacity factor, and the example of

representation of the mixing ratio may be 2:5:5 to 0.01:1:5. In addition, 29% and 31% of thing can be used for the concentration of the aqueous ammonia said here and hydrogen peroxide solution, respectively, for example.

[0026] both the capacity of washing and etching is [the one where the solution temperature at the time of washing of this invention is higher] high -- generally -- the temperature of 60 degrees C or more -- it is 60 degrees C - 95 degrees C more preferably.

[0027] In addition, an organic alkali system solution also has the capacity of silicon etching generally. For example, although TMAH (tetrapod methyl ammonium hydroxide) etc. is a phot lithography processes of a semiconductor device production line and is an ingredient currently widely used also as a developer of a photoresist, it is effective also as a penetrant remover of this invention.

[0028] Although there may be mixed liquor of fluoric acid and a nitric acid etc. as etchant of silicon, since a SOI front face, such as etching a crystal defect alternatively, may be damaged, at the time of use, cautions are required of this system.

[0029]

[Example] (The 1st example) One example of this invention is explained using drawing 2 and drawing 3 .

[0030] Drawing 2 is a mimetic diagram for explaining the production process using a porous layer and an epitaxial growth phase of a SOI wafer. Drawing 3 is the mimetic diagram showing anode plate degassing equipment. In drawing 3 , an electrode terminal for 102 to supply an anodization tub and for 103 supply [as for a substrate electrode holder and 105 / a reduced pressure adsorption pad and 106] the current for anodization for opening of a substrate electrode holder and 104, as for the electrolytic solution for anodization and 107,108 and 109 are reduced pressure Rhine.

[0031] First, specific resistance prepared the 8 inch device wafer which is 0.015-ohmcm with P type as a silicon substrate 1.

[0032] The front face of the device wafer 101 was contacted to the adsorption pad 104 of the electrode holder 103 placed into the anodization tub 102 in this device wafer 101, and by reduced pressure Rhine 109 connected to the adsorption slot (un-illustrating) of a pad 104, reduced pressure adsorption was carried out and it fixed.

[0033] To the tub 102, the mixed liquor of hydrofluoric-acid:ethanol =2:1 was filled with this condition as the electrolytic solution.

[0034] and formation -- between the minus electrodes 107 made from platinum and the plus electrodes 108 which were prepared in the both ends of a tub, it energized for 5 minutes and changed into the 2nd current value of 7.2A continuously with the 1st current value (2.5A) first, and energized for 1 minute. Consequently, from the front face of the device wafer 1 to a depth of 5 micrometers became the 1st porosity silicon layer 21, and the porous layer 2 which consists of two or more porous bodies from which even 2 more micrometer depth serves as the 2nd thin porosity silicon layer 22 which is the degree of Kota hole from the 1st porosity silicon layer, and porosity differs mutually in this way was formed.

[0035] Next, it oxidized thermally at 400 degrees C, and the thin oxide film was formed in the porous wall side of the 1st and 2nd porous layers 2. And after washing in a rare hydrofluoric acid, the device wafer was arranged on the CVD system, temperature was raised for hydrogen gas with the sink, and hydrogen BEKU of the porous layer 2 was carried out. Then, dichlorosilane (SiH_2Cl_2) was passed with hydrogen carrier gas, at 1050 degrees C, epitaxial growth was performed on the front face of the 1st porous layer 2, and the 150nm nonvesicular single-crystal-silicon film 3 (SOI layer) was formed in it (drawing 2 C).

[0036] Subsequently, the front face of the single-crystal-silicon film 3 was oxidized thermally, and the 100nm silicon oxide layer 4 was formed (drawing 2 R>2D). Formation of this silicon oxide layer is also omissible.

[0037] After washing the handle wafer 10 prepared independently, it stuck on the silicon oxide layer of a device wafer at the room temperature in the ambient atmosphere [****] (drawing 2 F). In addition, in case the SOI layer 3 (or silicon oxide layer 4 formed on it) of the device wafer 1 and the handle wafer 10 are stuck, and the device wafer may have the insulator layer on the

silicon substrate, or may be a light transmission family name substrate and an insulating film.
[that it is a silicon substrate]
[0038] after heat-treating this stuck wafer (multilayer-structure object) in 1100-degree C nitrogen-gas-atmosphere mind for 2 hours -- the side face of a wafer to ******** for lamination interfaces -- inserting -- two porosity silicon layers 21 and 22 -- in the interface, it dissociated about (drawing 2 G).
[0039] Thus, the wafer with which the silicon oxide layer 4 and the single-crystal-silicon film 3 were transferred by the handle wafer 10 was obtained. The porosity silicon layer 21 remained on the front face of the single-crystal-silicon film 3. (Drawing 2 G) .
[0040] next, this wafer -- hydrofluoric-acid: -- hydrogen-peroxide-solution: -- it dipped in the mixed liquor of water =1:20:50, and selective etching removed the porosity silicon layer 21 over the time amount for about 90 minutes, impressing a supersonic wave.
[0041] In order to make the front face of this wafer smooth, 1100-degree C hydrogen annealing was given for 1 hour, and the SOI wafer of 100nm of silicon layers and 100nm of embedding oxide films was obtained (drawing 2 H).
[0042] Then, in order to control more thinly the thickness of the single-crystal-silicon film (SOI layer) 3 of the obtained SOI wafer, 85 degrees C heated this SOI wafer. a presentation -- a capacity factor -- aqueous ammonia: -- hydrogen-peroxide-solution: -- it dipped in the SCI solution of water =0.05:1:10, and washed. Since it was a part for etching great ** [by this washing process], and 0.5nm/, washing was continued for 140 minutes and 70nm etching removal of the SOI layer 103 was carried out.
[0043] In addition, the concentration of aqueous ammonia is 31% of hydrogen peroxide solution 29%.
[0044] As a result, the super-thin film SOI wafer whose thickness of 30nm and an embedding silicon oxide layer the thickness of a SOI layer is 100nm was obtained.
[0045] When the front face of this SOI wafer was observed, it was a very smooth and uniform front face, without almost changing immediately after carrying out hydrogen annealing treatment.

[0046] <Comparative-experiments **> Comparative experiments with the case where wash like the case where it thin-film-izes by sacrifice oxidation, and this invention, and it is made thin were conducted.
[0047] Apart from the SOI wafer (sample A) which specifically washed as mentioned above with the mixed liquor of said aqueous ammonia / hydrogen peroxide solution / water, and etched 70nm of thickness, after about 150nm oxidized the SOI layer by thermal oxidation, the oxide film was etched in rare fluoric acid, and the SOI wafer (sample B) which reduced SOI thickness by about 70nm as a result was prepared.
[0048] In order to compare front-face nature of a SOI layer, after both were immersed in dark fluoric acid for 15 minutes, it performed observing the front face under a microscope.
[0049] Consequently, as for Sample B, about five voids (the opening under the SOI film formed since fluoric acid embedded through the defect of a SOI layer or the through tube, and the oxide-film layer was reached, it subsequently embedded and the oxide film was etched by fluoric acid: common-name HF void) /with a diameter of about 50 micrometers were observed by the consistency of 2 cm. On the other hand, in Sample A, 0.05 so-called consistencies /of HF void remained in 2 cm.
[0050] The crystal defect included in SOI in an oxidation process oxidizes in accelerating, the part is etched, it becomes very thin that whose Sample B, i.e., HF void consistency of the wafer oxidized thermally, was high, when it dips in HF solution, a hole is vacant as for it into a SOI part, and it is imagined as what HF void became is easy to be formed as for.
[0051] <Comparative-experiments **> In having depended and decrease of thickness made it above-mentioned "etching (1) of porosity silicon" "hydrogen annealing (2)" "washing, and deciding the sequence of (3)", it determined by conducting the following experiments. When the above-mentioned process was performed by (1) ->(3) -> (2) (this will perform flattening by hydrogen annealing after making the SOI film thin), as a result of performing this, when microscope observation of the wafer front face after hydrogen annealing was carried out, many

things considered to be square pits were observed. This is idea **** since the heat stress of annealing affected the very thin silicon film of 30nm, big stress concentrated by the crystal defect part or the part which was thin locally and the hole opened on the film under the annealing ambient atmosphere. Although the boundary of silicon and silicon oxide will be exposed if a hole opens, a reaction called Si+SiO2 ->2SiO in it occurs in a hydrogen ambient atmosphere, silicon and silicon oxide gasify, and a hole is expanded. For this reason, for production of a thin film SOI layer, SOI thickness finds out that it is necessary to anneal where it has thickness comparatively, and came to accomplish thin film-ized **** this invention in the sequence (1) -> (2) -> (3) to it.

[0052] When carrying out hydrogen annealing of the SOI layer, it is desirable that 70nm or more of thickness in the time is 100nm or more more preferably. However, it is not this limitation when an embedding oxide-film layer is thick enough. For example, when it has the thickness whose embedding oxide film is about 500nm, about 50nm is sufficient as the thickness of the SOI layer in front of hydrogen annealing. When the thickness of an embedding oxide film is about 100nm, as for the thickness of a SOI layer, it is good that it is 70nm or more.

[0053] (Formation of a porous layer) formation of a porous layer on a wafer front face -- anodization -- it can carry out -- current density and formation -- the class of solution or its concentration can be changed and two-layer [from which porosity differs mutually], or two or more porous layers of three or more layers can also be formed.

[0054] As for the configuration of a porous layer, it is especially desirable to have the 1st porous layer which has the 1st porosity from an outside front face, and the 2nd porous layer which has the 2nd larger porosity than this 1st porosity in this order. While being able to form a nonvesicular layer with few defects etc. (for example, nonvesicular single-crystal-silicon layer) on the 1st porous layer by the configuration concerned, it becomes separable in the location of a request of a porous layer.

[0055] As the 1st porosity, it is desirable that it is 15% - 25% more preferably 10% to 30%. Moreover, as the 2nd porosity, it is desirable that it is 40% - 60% more preferably 35% to 70%.

[0056] the formation for anodization -- as liquid, the solution containing hydrogen fluoride, the solution containing hydrogen fluoride and ethanol, the solution containing hydrogen fluoride and isopropyl alcohol, etc. can be used.

[0057] (Formation of a nonvesicular layer) It precedes forming a nonvesicular layer on a porous layer here, and at least one of the processes of following (b) - (d) can also be added. desirable -- (**) -- -> (**) -- more -- desirable -- (**) -- -> (**) -- -> (Ha) or (**) -- -> (**) -- -> (**) -- further -- desirable -- (**) -- -> (**) -- it is good to perform ->(Ha) -> (d) and a series of processes.

[0058] (b) You may prepare protective coats, such as an oxide film and a nitride, in the porous wall of the protective coat formation process porous layer to a porous wall, and may also prevent big and rough-ization of the hole by heat treatment. For example, it heat-treats by the oxidizing atmosphere (200 degrees C - 700 degrees C, preferably 300-500 degrees C). The oxide film formed on the surface of the porous layer at that time may be removed (for example, a front face is exposed to the solution containing HF.).

[0059] (b) It is also desirable to heat-treat at 800 degrees C - 1200 degrees C among the reducing atmosphere containing hydrogen in advance of formation of the nonvesicular layer to a hydrogen baking process porous layer top. While being able to close the hole on the front face of a porous layer to some extent by the heat treatment concerned, it is also possible to remove it when the natural oxidation film exists in a porous layer front face.

[0060] (c) When growing up a nonvesicular layer to be up to a minute amount feeding process porous layer, it is desirable to carry out minute amount supply of the source material of this nonvesicular layer in a growth initial stage, and to make it grow up with a low speed. migration primitive [on the front face of a porous layer] promotes with this growth -- having -- a hole -- a front face can be closed.

[0061] Below 20 nm/min., specifically, a growth rate adjusts feed below 10 nm/min. preferably so that it may become a growth rate below 2 nm/min. more preferably.

[0062] (d) Much more closure on the front face of a porous layer and smoothing are attained by

heat-treating in the reducing atmosphere which is temperature higher than the processing temperature in the hydrogen baking process and/or minute amount feeding process of the elevated-temperature baking process above-mentioned, and contains hydrogen.
[0063] Homoepitaxial growth or heteroepitaxial growth is possible for formation of the nonvesicular layer to a porous layer top. As a nonvesicular layer, Si, germanium, SiGe, SiC and C, GaAs, GaN, AlGaAs, InGaAs, InP, InAs, etc. are possible.
[0064] (The transfer approach of a nonvesicular layer) As an approach of transferring the nonvesicular layer formed in up to a porous layer to a support substrate or a film Grinding, polish, etching, or such combination remove the unnecessary nonvesicular section from the multilayer-structure object acquired from a lamination process. Etching (etchant: HF+H2O2 or HF+ alcohol, HF+H2O2+ alcohol) etc. removes the porous layer expressed after that, or there is a method of separating this multilayer-structure object by the porous layer.
[0065] Separation can be performed by applying pull strength, compressive force, shearing force, etc. to this multilayer-structure object, or spraying a fluid on this multilayer-structure object side face.
[0066] The liquid which has the operation which etches alternatively alkali and other isolation regions, such as acids, such as organic solvents, such as water and alcohol, and fluoric acid, a nitric acid, or a potassium hydroxide, as a fluid to be used is usable. A low-temperature cooling fluid and a super-cooling liquid can also be used. Furthermore, gases, such as air, nitrogen gas, carbon dioxide gas, and rare gas, may be used as a fluid.
[0067] When a porous layer remains on the nonvesicular layer transferred to up to a support substrate, etching and polish can remove. It is also possible to attain surface smoothing by heat treatment in a hydrogen ambient atmosphere.
[0068] In this way, the SOI wafer obtained is thin-film-ized using the approach by this invention.
[0069] (The 2nd example) With reference to drawing 4 , the manufacture approach of the silicon thin film by another example of this invention is explained.
[0070] Specific resistance prepared first the CZ silicon wafer 1 which is 8 inches which is 10-ohmcm with P type as a substrate (drawing 4 R>4A).
[0071] Homoepitaxial growth by CVD which used trichlorosilane (SiHCl3) for this wafer front face was performed, and the 10-micrometer epitaxial layer 5 was formed (drawing 4 B).
[0072] Then, the layer 7 which drives the oxygen ion 6 into this wafer front face by 2x1018/cm2 of doses and acceleration energy 180KeV, and contains oxygen ion by high concentration in the film of an epitaxial layer 5 was formed (drawing 4 C). As oxygen ion, it is O+.
[0073] In addition, it faces devoting oneself and insulator layers, such as an oxide film, may be formed on epitaxial layer 5 front face.
[0074] Next, this wafer was placed into the argon ambient atmosphere, heat treatment of 6 hours was performed at 1350 degrees C, and the high-concentration oxygen ion content layer 7 was changed to the silicon oxide layer 4. In this way, the thickness of the SOI layer 3 formed from epitaxially grown silicon was set to 190nm, and the thickness of the embedding silicon oxide layer 4 was set to 380nm.
[0075] This wafer was dipped in SC1 solution of the same presentation as the 1st example for 180 minutes, and was washed, and the SOI layer 3 was thin-film-ized to 100nm. The thickness homogeneity of this SOI layer was high, and that front face was also very smooth. In addition, the so-called ITOX method may be used for thick-film-izing of a pad oxide film.
[0076] (The 3rd example) With reference to drawing 5 , the manufacture approach of the silicon thin film by another example of this invention is explained.
[0077] Specific resistance prepared first the FZ silicon wafer 1 which is 6 inches which is 100-ohmcm with P type as a substrate (drawing 5 A).
[0078] Then, the layer 7 which drives the oxygen ion 6 into this wafer front face by 2x1018/cm2 of doses and acceleration energy 180KeV, and contains oxygen ion in the part below the front face of FZ wafer by high concentration was formed (drawing 5 B).
[0079] It heat-treated in the argon ambient atmosphere on the same conditions as the 2nd example, and the SOI wafer whose thickness of 190nm and the embedding silicon oxide layer 4 the thickness of the SOI layer 3 is 380nm was obtained.

[0080] Then, the SOI wafer was dipped in the HF concentration 5wt% hydrofluoric acid for 1 minute, the surface natural oxidation film was removed completely, and the pure-water rinse was fully carried out.
[0081] And the above-mentioned SOI wafer was dipped in the TMAH water solution whose TMAH concentration marketed as a developer is 2.35wt(s)%, the SOI layer 3 was washed for 20 minutes at the room temperature, and about 140nm of surfaces of the SOI layer 3 was removed. The etch rate of the silicon by this water solution was a part for about 7nm/in 25-degree-C solution temperature.
[0082] Then, the SOI wafer was washed for 5 minutes using the SC1 same solution as what was used in the 1st example.
[0083] Thereby, the SOI layer was able to be thin-film-ized from 190nm of origin to 50nm rather than the 2nd example in a short time.
[0084] (The 4th example) With reference to drawing 6 , the manufacture approach of the silicon thin film by another example of this invention is explained.
[0085] Specific resistance prepared first the 8 inch CZ wafer 1 which is 10-ohmcm with P type as a substrate.
[0086] This wafer was placed into the hydrogen ambient atmosphere, at 1200 degrees C, heat treatment of 6 hours was performed, the oxygen sludge near the wafer front face was returned, and the hypoxia concentration layer 8 which reduced the oxygen density was formed (drawing 6 B).
[0087] After this, like the 3rd example, the oxygen ion 6 was driven in and heat-treated (drawing 6 C), the embedding silicon oxide layer 4 was formed (drawing 6 D), etching and washing were performed to continuation after that, and the SOI wafer of the same thickness configuration as the 3rd example was obtained.
[0088] (The 5th example) The 6th example of this invention is explained using drawing 7 .
[0089] The silicon wafer 71 of 10-20ohms of 8inchp molds cm which are a device wafer first was prepared (drawing 7 A).
[0090] Subsequently, the 5-micrometer silicon layer 72 was grown up into the front face of 71 by the usual epitaxial method (drawing 7 B). In addition, this epitaxial growth process can also be skipped.
[0091] And the front face of this epitaxial silicon layer 72 was oxidized thermally, and the 400nm silicon oxidation membrane layer 73 was formed (drawing 7 C). In addition, this oxide-film layer formation process can also be skipped.
[0092] Next, the hydrogen ion was poured in from the front face of the silicon oxidation membrane layer 73 using ion implantation equipment (drawing 7 D). The impregnation energy and the dose at this time were set to 100keV(s) and 2x1015-/cm2, respectively. As a result, the hydrogen ion reached in about 800nm Fukashi from the substrate front face, and formed the ion-implantation layer 75. It is thought that distorted stress is applied to this ion-implantation layer. In addition, this ion-implantation layer may be formed in a silicon wafer 71, or may be formed near the interface of the silicon layer 72 and a silicon wafer 71.
[0093] Next, the silicon wafer 7 of 10-20ohms of 8inchp molds cm which are one more support wafer was prepared, and it stuck, after washing mutually the front face of this support wafer 7, and the front face (silicon oxidation membrane layer 73 front face) of the device wafer 71 (drawing 7 E). In order to raise lamination reinforcement before sticking here, each wafer was put on the plasma generator (un-illustrating), and actuation which puts nitrogen ion to a front face was performed. Compared with the case of only only washing lamination reinforcement and sticking, one about 5 times the lamination reinforcement of this was obtained in the room temperature by this actuation.
[0094] After performing 300 degrees C and heat treatment of 1 hour to the stuck substrate and making lamination reinforcement still firmer, the air-jet nozzle 77 was close brought near the lamination interface, and the compressed air 78 was sprayed on it by the pressure of 6kg/cm2. As a result, separation took place within the layer of the ion-implantation layer 75 by the side of the device wafer 71, and the device wafer 71 and support wafer 76 side dissociated completely bordering on the ion-implantation layer 75 (drawing 7 F). In addition, the tip configuration of the

air-jet nozzle 77 used on this occasion was making the rectangle whose cross section is 0.1mmx6mm, when it sprayed air, brought the tip of a nozzle close to the location of 1mm from the substrate lamination interface, and went.

[0095] Consequently, the SOI structure of having had about 350nm epitaxial silicon layer 72 the 400nm silicon oxidation membrane layer 73 and on it, and having about 50nm ion-implantation layer 75 on it on the support wafer 76 was acquired (drawing 7 G).

[0096] Then, 1050 degrees C and hydrogen annealing treatment of 3 hours are performed to the obtained SOI wafer, and the very smooth condition was made to reform the front face it was ruined with separation at the same time it removed the strain of the ion-implantation layer 75.

[0097] The silicon epitaxial layer (SOI layer) 72 which became smooth at the end was dipped in the same developer as the 2nd example, and washing ******** was performed. The developer in this case uses what heated the 2.35wt(s)% TMAH solution at 80 degrees C. By dipping in SC-1 liquid further used in the 1st example by dipping for 4 minutes into this liquid for 20 minutes, 320nm 10nm, Total a wafer of 330nm SOI which washes by **** carrying out and has the 70nm silicon epitaxial layer (SOI layer) 2 and the 400nm silicon oxidation membrane layer (embedding oxide-film layer) 3 as a result was completed.

[0098] In addition, the ion-implantation kinds for isolation region formation are rare gas, such as hydrogen and helium. Moreover, ion-implantation can be poured in in the shape of a beam, or plasma immersion ion-implantation (PIII technique) can be used for it. As a fluid to spray, you may be gases, such as nitrogen and an argon, besides air. About these things, it is detailed in the international public presentation official reports 98/52216.

[0099] (The manufacture approach of a semiconductor device) With reference to drawing 8 , the semiconductor device using the semi-conductor base by each operation gestalt and its manufacture approach of this invention explained above are described.

[0100] The SOI wafer 50 formed in the above-mentioned example 1 - 7 grades using this invention of a publication as a semi-conductor base is prepared.

[0101] Patterning of the SOI layer which consists of a nonvesicular semi-conductor on the embedding insulator layer 52 on a base material 51 is carried out to the shape of an island, or LOCOS oxidization is given, and the pattern 53 of the SOI layer of the field which should form a transistor is formed. By a diagram, the situation at the time of using the component isolation regions 54, such as an insulator, is mentioned as an example, and is shown.

[0102] Gate dielectric film 56 is formed in the front face of the SOI layer 53. As gate dielectric film 56, silicon oxide, silicon nitride, oxidization silicon nitride, an aluminum oxide, tantalum oxide, an oxidization hafnium, titanium oxide, oxidization SUTANJIUMU, an oxidization yttrium, an oxidization gadolinium, lanthanum oxide, zirconium dioxides, these mixture glass, etc. are used. This gate dielectric film 56 can be formed by oxidizing or depositing the front face of the SOI layer 53 on the front face of the SOI layer 53 by CVD or PVD.

[0103] The gate electrode 55 is formed on gate dielectric film 56. As a gate electrode 55, metal nitrides, such as metal silicides, such as metals (the alloy containing at least one sort of these is ncluded), such as polycrystalline silicon with which P type or an N type impurity was doped, and a tungsten, molybdenum, titanium, a tantalum, aluminum, copper, and molybdenum silicide, ungsten silicide, cobalt silicide, and titanium night RAIDO, tungsten night RAIDO, tantalum night AIDO, are used. Two or more kind laminating of the layer of these ingredients may be carried ut like the polycide gate, and it may be used. Here, although the case where a gate electrode is rmed in the process called Salicide (self aryne silicide) is described, you may form by the proach called a DAMASHIN gate process.

104] In this way, the structure as shown in drawing 8 (a) is obtained.

105] After forming the pattern of the gate electrode 55, P type impurities, such as N type urities, such as Lynn, arsenic, and antimony, or boron, are introduced into the SOI layer 53, the comparatively low-concentration source and the drain field 58 which were adjusted on side face of the gate electrode 55 are formed. An impurity can be introduced by ion lantation, heat treatment, etc.

06] After forming an insulator layer so that the gate electrode 55 may be covered, etchback arried out and the side wale 59 is formed in the side face of the gate electrode 55.

[0107] The impurity of the again same conductivity type is introduced and the comparatively high-concentration source drain field 57 adjusted in the sidewall 59 is formed.
[0108] In this way, the structure shown in drawing 8 (b) is obtained.
[0109] A gate electrode top face and the top face of a source drain field are exposed, and the layer 60 of a metal semiconducting compound is formed there. As a metal semiconducting compound, metal silicide is desirable and nickel silicide, titanium silicide, cobalt silicide, molybdenum silicide, tungsten silicide, etc. are specifically used. Such silicides make a metal deposit so that the top face of the gate electrode 55 and the top face of the source drain field 57 may be covered, and after heat-treating and making it react with the silicon of the source drain field 57, they can be formed by removing a metaled unreacted part by etchant, such as a sulfuric acid. The front face of the layer 60 of a metal semiconducting compound may be nitrided further if needed.
[0110] In this way, the structure shown in drawing 8 (c) is obtained.
[0111] An insulator layer 61 is formed so that the gate electrode top face and source drain field top face which were silicide-ized may be covered. As this insulator layer 61, the silicon oxide containing Lynn and/or boron etc. is used preferably.
[0112] If needed, flattening of the top face of an insulator layer 61 is carried out by etchback or CMP, and a contact hole is formed in an insulator layer 61. If the photolithography which makes the light source KrF excimer laser, ArF excimer laser, F2 excimer laser, an electron beam, and an X-ray is used, the contact hole of a rectangle with one side of die length smaller than 0.25 microns or a circular contact hole with a diameter with one side of die length smaller than 0.25 microns can be formed.
[0113] A conductor plug is formed in a contact hole. After forming at least one layer which consists of the refractory metal film, metal semiconducting compounds, or refractory metal nitrides used as the barrier metal 62 as the formation approach of the conductor plug in a contact hole, the electrical conducting materials 63, such as a tungsten, a tungsten alloy, aluminum and an aluminium alloy, copper, and a copper alloy, are made to deposit using CVD, PVD, and plating, and etchback and CMP may remove the electrical conducting material which is above an insulator layer top face if needed.
[0114] Or after nitriding the front face of the silicide layer 60 of the source drain field 57 exposed from the contact hole if needed, it may be filled up with a conductor in a contact hole.
[0115] In this way, the structure (MOS mold thin film transistor) as shown in drawing 8 (d) is obtained.
[0116] In this way, semiconductor devices, such as a transistor, can be manufactured using the SOI wafer of this invention.
[0117] If it determines that the depletion layer which impresses an electrical potential difference to a gate electrode, and spreads under gate dielectric film at this time embeds, and the thickness and high impurity concentration of a SOI layer reach the top face of an insulator layer, this transistor will operate as a perfect depletion mold transistor. Moreover, if it determines that a depletion layer embeds and the thickness and high impurity concentration of a SOI layer do not reach the top face of an insulator layer, this transistor will operate as a partial depletion mold transistor.
[0118] Since thin-film-izing of a SOI layer is possible when this invention is used, formation of a perfect depletion mold transistor becomes easy.
[0119]
[Effect of the Invention] According to this invention, degradation of the oxide-film pressure-proofing accompanying the surface dry area under accelerating oxidation of the crystal defect section produced when performing the conventional sacrifice oxidation, the effect of a foreign matter, etc., and a surface dry area etc. is avoidable. Moreover, a thermal oxidation process and the etching process of the thermal oxidation film can be skipped. In this way, it becomes possible to form in uniform thickness about the SOI wafer of a super-thin shape (100nm or less) which was difficult to create directly until now, without damaging a front face.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the approach of controlling the thickness of the silicon thin film used for a SOI wafer etc., and the manufacture approach of a silicon thin film about the manufacture approach of a silicon thin film. Silicon thickness is decreased by wet washing and, more specifically, it belongs to the technical field which obtains the thickness of arbitration.

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PRIOR ART

[Description of the Prior Art] as the manufacture approach of a SOI wafer -- SIMOX (Separetion by IMplanteion of OXygen) -- law, a lamination method, etc. are learned.
[0003] The SIMOX method is a technique which forms a silicon oxide layer in the location which drove in oxygen ion from the front face of a silicon substrate, and was embedded by subsequent elevated-temperature annealing. The dose of impregnation energy ** of the oxygen ion at this time cannot be set to arbitration, but is set to about certain conditions. Therefore, the SOI wafer which can come to hand can change neither silicon thickness nor thickness of an embedding oxide film into arbitration easily.
[0004] There are some classes of lamination methods. The approach currently called "the lamination polish SOI" etc. is mentioned first.
[0005] It is the approach of preparing two wafers with which at least one side oxidized, grinding these with grinding from one side at a room temperature after annealing, lamination and, and leaving the silicon thickness of arbitration on a silicon oxide layer. By this approach, the thickness of a silicon layer and the thickness of an embedding silicon oxide layer can be set as arbitration. However, in order to depend for thin film-ization of a silicon layer only on grinding and polish, the thin film of hundreds of nm uniform thickness is difficult to get by the limitation of the original thickness precision of a silicon wafer, and the precision of polish.
[0006] In order to compensate the above-mentioned fault, distribution of SOI thickness is measured in an instant, dry etching of the field and thinner is carried out few, and the technique which forms a super-thin film (100nm or less) in homogeneity is reported. [field / thicker] This technique was called PACE (Plasma Assisted Chemical Etching) and is divided into the unit which carries out field Uchida point (10000 or more points) measurement of the SOI thickness in an instant as mentioned above, and the unit which carries out plasma etching. To the unit of etching, it has the plasma generating part of a nozzle mold, and it can move now along a field in the upper part of a wafer side so that the nozzle can etch more thick fields according to the measurement result of the thickness of a SOI layer. The amount of etching is controlled for every field within a wafer side, and the absolute value of thickness and homogeneity can be controlled. However, in order that an etching damage may remain in the front face by which plasma etching was carried out, polish for finally removing a damage layer is performed in many cases. Thickness which became homogeneity with much trouble by this action may be ununiformity-ized again.
[0007] moreover, the front face of the silicon wafer which the oxide film attached as another lamination method as it was in a U.S. Pat. No. 5374567 number -- a hydrogen ion -- pouring in -- the interior of a wafer -- a brittle layer -- forming -- heating of an another wafer and lamination after that, and after that -- or there are some which spray a fluid (gases, such as liquids, such as water, or nitrogen) on a lamination wafer side face, dissociate from a brittle layer, and acquire SOI structure.
[0008] Control of thickness is controllable by the thickness of the oxide film of the wafer prepared first, the impregnation energy of a hydrogen ion, etc. However, to the dry area on the separated front face of SOI, polish finishing is needed in many cases and, thereby, thickness will become an ununiformity.

[0009] Moreover, as another lamination method, there is an approach indicated by a U.S. Pat. No. 5371037 number (patent No. 2608351), JP,5-21338,A, or JP,7-302889,A. This approach is an approach of removing an another wafer and lamination, and an unnecessary part for the silicon single crystal film which grew epitaxially on the substrate which has porosity silicon through an oxide film, and obtaining a SOI layer. Control of the thickness in this approach is made by control of epitaxial thickness and oxide-film thickness etc.

[0010] Although it may be ruined at the process which carries out selective etching of the porosity silicon which remains on a SOI layer front face if the front face after a process is observed, it is carrying out hydrogen annealing of the SOI layer front face as indicated by JP,5-218053,A, and is made in a very smooth field. According to this approach, degradation of distribution of the thickness of a SOI layer does not take place.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, degradation of the oxide-film pressure-proofing accompanying the surface dry area under accelerating oxidation of the crystal defect section produced when performing the conventional sacrifice oxidation, the effect of a foreign matter, etc., and a surface dry area etc. is avoidable. Moreover, a thermal oxidation process and the etching process of the thermal oxidation film can be skipped. In this way, it becomes possible to form in uniform thickness about the SOI wafer of a super-thin shape (100nm or less) which was difficult to create directly until now, without damaging a front face.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, even if it is these lamination methods, it is not easy for thickness to form a super-thin film 100nm or less directly, for example.
[0012] In order to remove the etching damage layer of the plasma which remains in a front face in the case of the PACE method, it is necessary to make a thicker SOI layer a little in consideration of a part for the thickness. However, since the damage layer removal is performed by polish, the thickness distribution variation by polish occurs and homogeneity formation of a super-thin film becomes difficult. By the approach which needs polish of a SOI layer for the same reason, direct formation of a super-thin film becomes difficult altogether.
[0013] Moreover, when the above-mentioned hydrogen annealing is used for smoothing of the SOI film, a pinhole may occur. It exists in a lamination interface. In a measuring instrument, stress is applied to the minute field by the side of the lamination interface of a super-thin film that it cannot measure with such a minute (90nm or less) foreign matter and the surface irregularity of the wafer itself. Under existence of this stress, if hydrogen annealing treatment is performed, a pinhole may occur to a stress generating part. On the other hand, in the case of the design of semiconductor devices, such as a transistor, when the SOI thickness demanded is still thinner than the minimum thickness which can be supplied as a SOI wafer, or when the SOI wafer of different thickness with modification of a design is needed, a wafer supply side cannot fully respond. In such a case, once the manufacturer of a semiconductor device receives beforehand the SOI wafer with a SOI layer thicker than design thickness and oxidizes the front face thermally, he has to perform sacrifice oxidization of removing the part which oxidized by etching, and has to get the SOI layer of desired thickness.
[0014] However, if sacrifice oxidation is performed, the accelerating oxidation over the crystal defect which exists in the SOI film has done enough, and since oxidation is checked around the field where the foreign matter adhered, the surface dry area of the front face of a SOI layer will be caused as a result. This becomes the cause of degrading oxide-film pressure-proofing of a semiconductor device.

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MEANS

[Means for Solving the Problem] The purpose of this invention is to offer the thickness control approach of a silicon thin film that the value of a request of the thickness can be decreased, the manufacture approach of a silicon thin film, and the manufacture approach of a SOI substrate, without degrading the quality of a silicon thin film.
[0016] In the manufacture approach of the silicon thin film for manufacturing the silicon thin film prepared on the insulating front face, by carrying out wet washing of the silicon thin film prepared on said insulating front face, this invention is characterized by including the process which decreases the thickness of this silicon thin film until it becomes thickness 100nm or less. Moreover, the manufacture approach of the silicon thin film concerning this invention of the 1st thickness of said silicon thin film before [said] carrying out wet washing is larger than 100nm, and it is characterized by performing this wet washing after heat-treating this silicon thin film that has this 1st thickness in the reducing atmosphere containing hydrogen until it becomes the 2nd thickness thinner than this 1st thickness. For example, said 2nd thickness is 100nm or less or 50nm or less.
[0017] The creation approach of the SOI substrate concerning this invention is characterized by to include the process which carries out wet washing of this base after the process which prepares the base which has the silicon thin film of the 1st larger thickness than 100nm on an insulating front face, the heat treatment process which heat-treats this base in the reducing atmosphere containing hydrogen, and this heat treatment process, and makes this silicon thin film the thickness of the 2nd thickness thinner than this 1st thickness.
[0018] After said base sticks the 1st substrate and 2nd substrate which have a silicon thin film through an insulating layer and forms a compound member on a porous layer, After being formed including the process which separates this compound member by the porous layer, or sticking the 1st substrate and 2nd substrate which have a silicon thin film through an insulating layer and forming a compound member on an ion-implantation layer, it is formed including the process which separates this compound member in this ion-implantation layer.
[0019] According to this invention, degradation of the oxide-film pressure-proofing accompanying the surface dry area under accelerating oxidation of the crystal defect section produced when performing the conventional sacrifice oxidation, the effect of a foreign matter, etc., and a surface dry area etc. is avoidable. Moreover, a thermal oxidation process and the etching process of the thermal oxidation film can be skipped.
[0020]
[Embodiment of the Invention] In this invention, as first shown in drawing 1 , the SOI substrate 50 is prepared, and wet washing is carried out, without oxidizing thermally the silicon thin film (SOI layer) 3 on the insulating layer 4 of the SOI substrate. The thickness of a SOI layer is made to decrease by this wet washing, and desired thickness is obtained. In addition, 10 is bases, such as silicon.
[0021] If it considers as the SOI layer used for this invention, the SOI layer of the SOI wafer produced by the SIMOX method mentioned above and the lamination method is desirable. and the SOI layer formed using the silicon thin film formed of epitaxial growth or hydrogen annealing or FZ (floating zone) -- CZ (CHOKURARU skiing) with the common SOI layer produced using the

silicon substrate formed of law -- since oxygen content is low, it is more desirable than the silicon wafer formed of law. Moreover, a MCZ wafer is also desirable. In this way, the obtained SOI layer does not have sludges, such as silicon oxide, into it, and serves as a homogeneous silicon thin film. As a substrate which directs a silicon thin film, an insulator layer is the substrate or insulator substrate of the semi-conductor formed in the front face, or ******.

[0022] It is because uniform oxidization and uniform etching in the part will be checked if matter other than silicon deposits in a silicon thin film.

[0023] CZ (CHOKURARU skiing) -- when the silicon wafer obtained in law is used as a SOI layer, a defect will occur in silicon by deposit of oxygen, or a surface dry area will arise. The oxygen that in CZ silicon wafer contained is returned by hydrogen, the concentration becomes low, and a deposit is suppressed. [many] Therefore, after forming a SOI layer as a SOI layer by which hydrogen annealing was carried out, without giving hydrogen annealing, hydrogen annealing may be given to the SOI layer and a SOI layer may be formed using the silicon wafer which carried out hydrogen annealing.

[0024] The thickness of the SOI layer before reducing thickness by this invention is larger than 100nm, and the thickness of the SOI layer finally obtained is the very thin film of 100nm or less.

[0025] As a penetrant remover used for this invention, SC1 penetrant remover used by the so-called RCA washing is suitable. SC1 penetrant remover is NH4OH and H2O2. It consists of mixed liquor of H2O. 1:5:5, 1:10:10, 0.05:1:5, 0.05:1:10, etc. may have standard aqueous ammonia, hydrogen peroxide solution, and various water at a capacity factor, and the example of representation of the mixing ratio may be 2:5:5 to 0.01:1:5. In addition, 29% and 31% of thing can be used for the concentration of the aqueous ammonia said here and hydrogen peroxide solution, respectively, for example.

[0026] both the capacity of washing and etching is [the one where the solution temperature at the time of washing of this invention is higher] high -- generally -- the temperature of 60 degrees C or more -- it is 60 degrees C - 95 degrees C more preferably.

[0027] In addition, an organic alkali system solution also has the capacity of silicon etching generally. For example, although TMAH (tetrapod methyl ammonium hydroxide) etc. is a phot lithography processes of a semiconductor device production line and is an ingredient currently widely used also as a developer of a photoresist, it is effective also as a penetrant remover of this invention.

[0028] Although there may be mixed liquor of fluoric acid and a nitric acid etc. as etchant of silicon, since a SOI front face, such as etching a crystal defect alternatively, may be damaged, at the time of use, cautions are required of this system.

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EXAMPLE

[Example]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a mimetic diagram for explaining this invention.
[Drawing 2] It is a mimetic diagram for explaining the manufacture approach of the silicon thin film by 1 operation gestalt of this invention.
[Drawing 3] It is the mimetic diagram showing anode plate degassing equipment.
[Drawing 4] It is a mimetic diagram for explaining the manufacture approach of the silicon thin film by the operation gestalt of this invention.
[Drawing 5] It is a mimetic diagram for explaining the manufacture approach of the silicon thin film by the operation gestalt of this invention.
[Drawing 6] It is a mimetic diagram for explaining the manufacture approach of the silicon thin film by the operation gestalt of this invention.
[Drawing 7] It is a mimetic diagram for explaining the manufacture approach of the silicon thin film by the operation gestalt of this invention.
[Drawing 8] It is a mimetic diagram about the manufacture approach of the semiconductor device using the SOI wafer produced by this invention.
[Description of Notations]
1 Silicon Substrate
2 Detached Core
3 Silicon Thin Film
4 Silicon Oxide Layer

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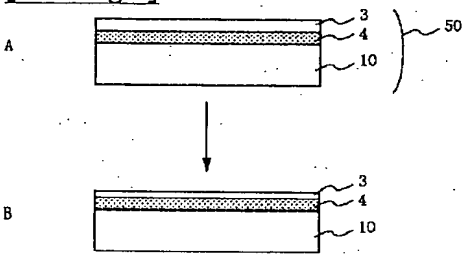
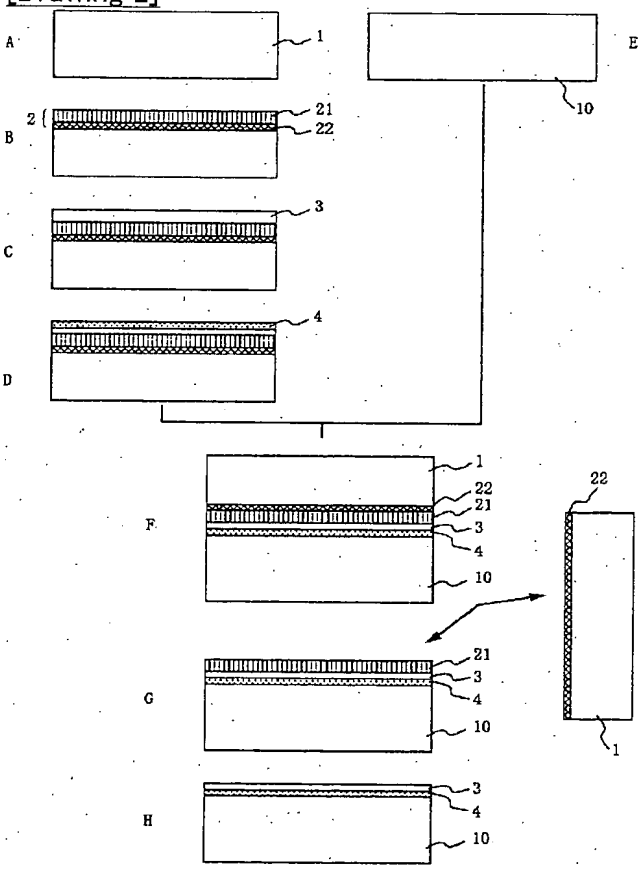
DRAWINGS

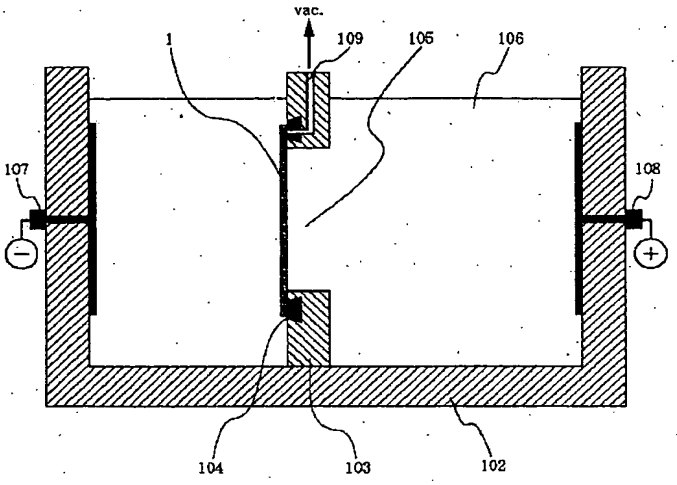
[Drawing 1]



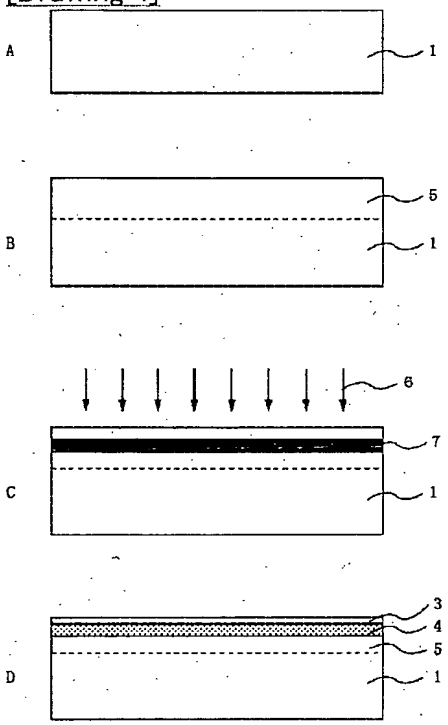
[Drawing 2]



[Drawing 3]



[Drawing 4]



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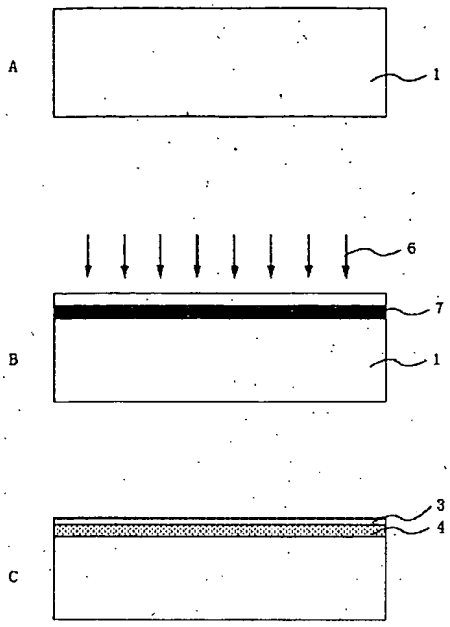

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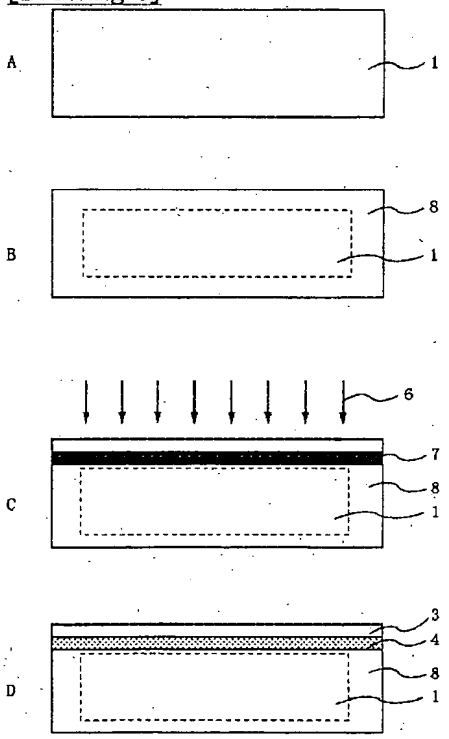

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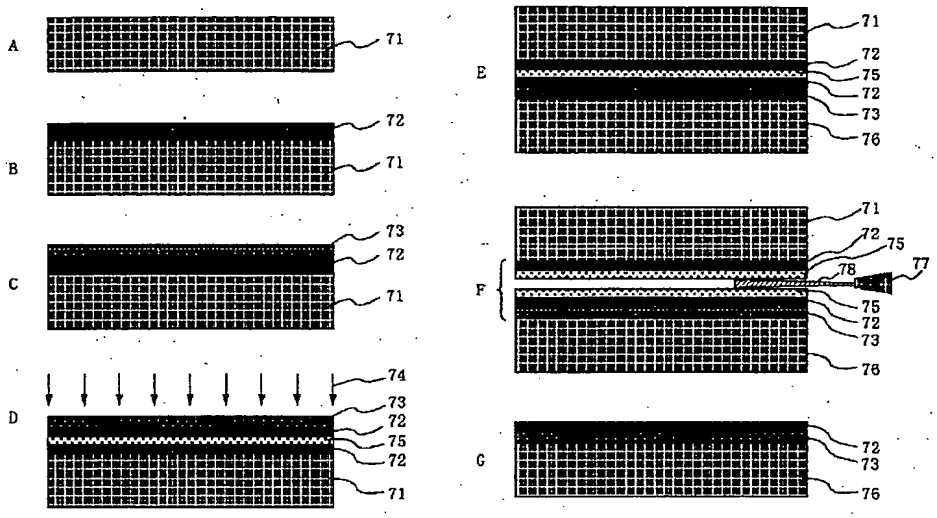

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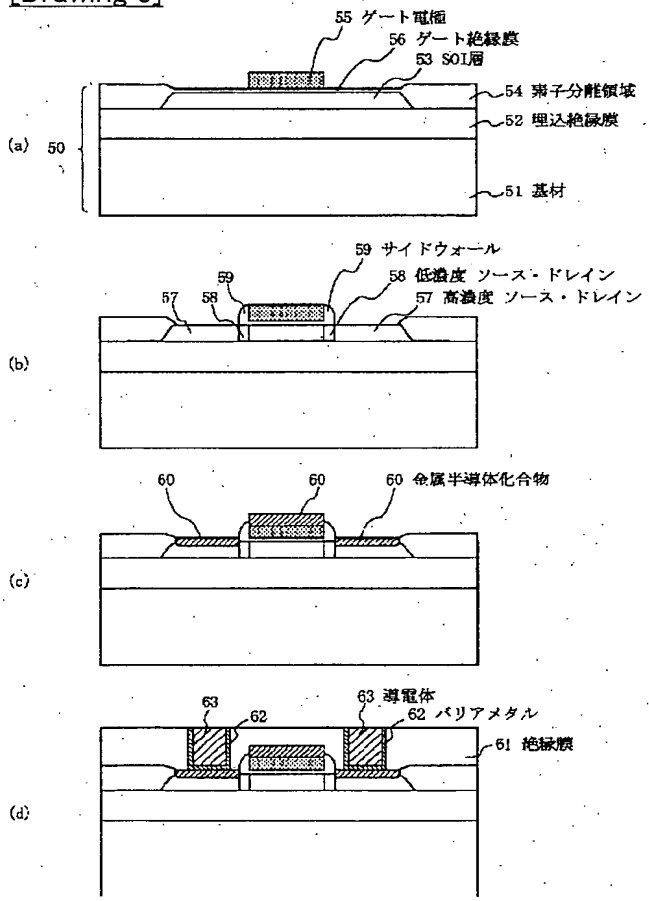

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号
特開2001－168308
（P2001－168308A）
(43)公開日　平成13年６月22日(2001.6.22)

(51)Int.Cl.[7]	識別記号	ＦＩ		テーマコード（参考）
Ｈ０１Ｌ　27/12		Ｈ０１Ｌ　27/12	Ｂ	
			Ｅ	
21/306		21/306	Ｂ	
29/786		29/78	６１８Ｄ	

審査請求　未請求　請求項の数23　ＯＬ　（全 12 頁）

(21)出願番号　特願2000－288734(P2000－288734)
(22)出願日　平成12年９月22日(2000.9.22)
(31)優先権主張番号　特願平11－278937
(32)優先日　平成11年９月30日(1999.9.30)
(33)優先権主張国　日本（ＪＰ）

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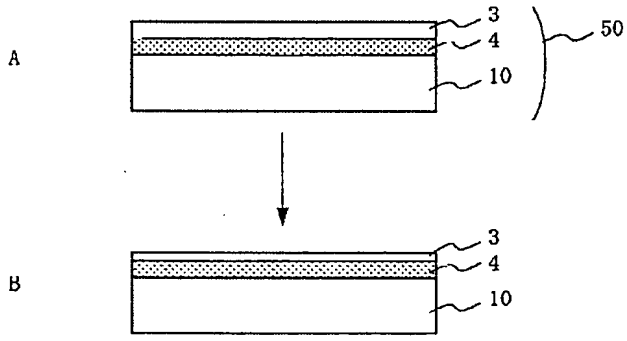
(54)【発明の名称】　シリコン薄膜の製造方法、ＳＯＩ基板の作製方法及び半導体装置

(57)【要約】
【課題】　従来の犠牲酸化を行う際に生じた結晶欠陥部の増速酸化や、異物の影響などによる表面荒れ、表面荒れに伴う酸化膜耐圧の劣化などを回避しつつ、シリコン薄膜の品質を劣化させることなく、その膜厚を所望の値に減少させる。
【解決手段】　ＳＩＭＯＸ法や貼り合せ法により、酸素析出物の少ないシリコン薄膜を有するＳＯＩウェハーを用意し、これをＳＣ１やＴＭＡＨなどのアルカリ溶液で洗浄し、この洗浄液のエッチング作用により、シリコン超薄膜ＳＯＩを製造する。



【特許請求の範囲】

【請求項１】　絶縁性表面上に設けられたシリコン薄膜を製造するためのシリコン薄膜の製造方法において、前記絶縁性表面上に設けられたシリコン薄膜をウェット洗浄することにより、１００ｎｍ以下の膜厚になるまで該シリコン薄膜の膜厚を減少させる工程を含むことを特徴とするシリコン薄膜の製造方法。

【請求項２】　前記ウェット洗浄する前の前記シリコン薄膜の第１の厚さは、１００ｎｍより大きく、該第１の厚さを有する該シリコン薄膜を水素を含む還元性雰囲気中で熱処理した後、該第１の厚さよりも薄い第２の厚さになるまで該ウェット洗浄を行うことを特徴とする請求項１記載のシリコン薄膜の製造方法。

【請求項３】　前記第２の厚さが５０ｎｍ以下である請求項２記載のシリコン薄膜の製造方法。

【請求項４】　前記シリコン薄膜は、エピタキシャル成長膜から得られたものである請求項１に記載のシリコン薄膜の製造方法。

【請求項５】　前記シリコン薄膜は、水素アニールされたシリコンから得られたものである請求項１に記載のシリコン薄膜の製造方法。

【請求項６】　前記シリコン薄膜は、ＦＺシリコンウエハから得られたものである請求項１に記載のシリコン薄膜の製造方法。

【請求項７】　前記ウェット洗浄は、ＳＣ１洗浄液又は有機アルカリ溶液を用いた洗浄である請求項１に記載のシリコン薄膜の製造方法。

【請求項８】　前記ウェット洗浄によるエッチング速度は０．１ｎｍ／分以上１０ｎｍ／分以下である請求項１に記載のシリコン薄膜の製造方法。

【請求項９】　前記シリコン薄膜は、熱酸化されることなく、ウェット洗浄処理に供される請求項１に記載のシリコン薄膜の製造方法。

【請求項１０】　前記シリコン薄膜は、ＣＺウエハより酸素含有率が低いシリコン膜からなる請求項１に記載のシリコン薄膜の製造方法。

【請求項１１】　前記ウェット洗浄は、アンモニアと過酸化水素とを含む洗浄液を用いた洗浄である請求項１に記載のシリコン薄膜の製造方法。

【請求項１２】　絶縁性表面上に１００ｎｍより大きい第１の厚さのシリコン薄膜を有する基体を用意する工程、該基体を水素を含む還元性雰囲気中で熱処理する熱処理工程、及び該熱処理工程の後、該基体をウェット洗浄し、該シリコン薄膜を該第１の厚さより薄い第２の厚さの膜厚にする工程を含むことを特徴とするＳＯＩ基板の製造方法。

【請求項１３】　前記基体が、多孔質層上にシリコン薄膜を有する第１の基板と第２の基板を絶縁層を介して貼り合わせて複合部材を形成した後、該複合部材を多孔質層で分離する工程を含み形成される請求項１２記載のＳＯＩ基板の作製方法。

【請求項１４】　前記基体が、イオン注入層上にシリコン薄膜を有する第１の基板と第２の基板を絶縁層を介して貼り合わせて複合部材を形成した後、該複合部材を該イオン注入層で分離する工程を含み形成される請求項１２記載のＳＯＩ基板の作製方法。

【請求項１５】　前記第１の基板は、シリコンウエハに水素イオンを所定の領域に注入する工程を含み形成される請求項１２記載のＳＯＩ基板の作製方法。

【請求項１６】　前記基体は、シリコンウエハに酸素イオンを注入する工程を含み形成されている請求項１２記載のＳＯＩ基板の製造方法。

【請求項１７】　前記第２の厚さが、５０ｎｍ以下である請求項１２記載のＳＯＩ基板の作製方法。

【請求項１８】　請求項１乃至１１に記載のシリコン薄膜の製造方法により製造されたシリコン薄膜。

【請求項１９】　請求項１２乃至１７に記載の方法により作製されたＳＯＩ基板。

【請求項２０】　請求項１２記載の前記シリコン薄膜にトランジスタの活性領域を形成することを特徴とする半導体装置の製造方法。

【請求項２１】　請求項１２記載の前記シリコン薄膜にトランジスタの活性領域が形成されていることを特徴とする半導体装置。

【請求項２２】　前記トランジスタは部分空乏型の薄膜ＭＯＳトランジスタである請求項１９に記載の半導体装置。

【請求項２３】　前記トランジスタは完全空乏型の薄膜ＭＯＳトランジスタである請求項２０に記載の半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、シリコン薄膜の製造方法に関し、特にＳＯＩウエハー等に用いられるシリコン薄膜の膜厚を制御する方法及びシリコン薄膜の製造方法に関する。より具体的には、シリコン膜厚をウェット洗浄によって減少させ、任意の膜厚を得る技術分野に属するものである。

【０００２】

【従来の技術】ＳＯＩウェハーの製造方法としては、ＳＩＭＯＸ（Ｓｅｐａｒｅｔｉｏｎ　ｂｙ　ＩＭｐｌａｎｔｅｉｏｎ　ｏｆ　ＯＸｙｇｅｎ）法、貼り合わせ法などが知られている。

【０００３】ＳＩＭＯＸ法は、シリコン基板の表面から酸素イオンを打ち込み、その後の高温アニールにより埋め込まれた位置に酸化シリコン層を形成する技術である。この時の酸素イオンの注入エネルギーやのドーズ量は、任意には設定できず、およそ一定の条件に定められている。従って入手できるＳＯＩウェハーは、シリコン膜厚や埋め込み酸化膜の膜厚を任意に変更し難い。

【0004】貼り合わせ法には、いくつかの種類がある。まず最初に挙げられるのは、「貼り合わせ研磨ＳＯＩ」などと呼ばれている方法である。

【0005】少なくとも一方が酸化された２枚のウェハーを用意し、これらを室温で貼り合わせ、アニールした後に片側から研削と研磨を行ない、任意のシリコン膜厚を酸化シリコン層の上に残す方法である。この方法ではシリコン層の厚み、埋め込み酸化シリコン層の厚みは任意に設定できる。しかしシリコン層の薄膜化を研削及び研磨のみに頼るために、シリコンウエハーの元の厚み精度、研磨の精度の限界により、数百ｎｍの均一な膜厚の薄膜が得難い。

【0006】上記欠点を補うためにＳＯＩ膜厚の分布を瞬時に測定し、厚めの領域を多く、薄めの領域を少なくドライエッチングし、超薄膜（１００ｎｍ以下）を均一に形成する技術が報告されている。この技術はＰＡＣＥ（Ｐｌａｓｍａ　Ａｓｓｉｓｔｅｄ　Ｃｈｅｍｉｃａｌ　Ｅｔｃｈｉｎｇ）と呼ばれ、前述したようにＳＯＩ膜厚を瞬時に面内多点（１００００点以上）測定するユニットと、プラズマエッチングするユニットに分かれている。エッチングのユニットにはノズル型のプラズマ発生部位を擁し、そのノズルがＳＯＩ層の膜厚の測定結果に従って厚い領域をより多くエッチングできるように、ウェハー面の上方を面に沿って移動できるようになっている。ウエハ面内の各領域毎にエッチング量を制御し、膜厚の絶対値と均一性を制御できる。但しプラズマエッチングされた表面にはエッチングダメージが残るため、最後にダメージ層を除去するための研磨を行なう場合が多い。この行為によりせっかく均一になった膜厚が再び不均一化される場合がある。

【0007】また別の貼り合わせ法として、米国特許５３７４５６７号にあるように酸化膜のついたシリコンウエハーの表面に水素イオンを注入し、ウェハー内部に脆弱層を形成し、その後別のウエハーと貼り合わせ、その後の加熱によりあるいは貼り合わせウエハ側面に流体（水などの液体、あるいは窒素などの気体）を吹きつけ脆弱層から分離してＳＯＩ構造を得るものがある。

【0008】膜厚の制御は最初に準備するウェハーの酸化膜の厚みや、水素イオンの注入エネルギー等で制御できる。但し、分離したＳＯＩ表面の荒れに対して、研磨仕上げが必要とされる場合が多く、これにより膜厚が不均一になってしまう。

【0009】また別の貼り合わせ法としては、米国特許５３７１０３７号（特許第２６０８３５１号）や特開平５－２１３３８号公報或いは特開平７－３０２８８９号公報に記載された方法がある。この方法は、多孔質シリコンを有する基板上にエピタキシャル成長したシリコン単結晶膜を、酸化膜を介して別のウェハーと貼り合わせ、不要な部分を除去して、ＳＯＩ層を得る方法である。この方法における膜厚の制御は、エピタキシャル膜厚、酸化膜厚の制御等でなされる。

【0010】ＳＯＩ層表面に残存する多孔質シリコンを選択エッチングする工程で、工程後の表面を観察すると荒れていることがあるが、それは特開平５－２１８０５３号公報に記載されているようにＳＯＩ層表面を水素アニールすることで、極めて平滑な面にできる。この方法によれば、ＳＯＩ層の膜厚の分布の劣化は起こらない。

【0011】

【発明が解決しようとする課題】しかしながら、これらの貼り合わせ法であっても、例えば厚さが１００ｎｍ以下の超薄膜を直接形成することは容易ではない。

【0012】ＰＡＣＥ法の場合、表面に残るプラズマのエッチングダメージ層を除去するため、その厚み分を考慮した若干厚めのＳＯＩ層を作る必要がある。しかし、そのダメージ層除去は研磨で行なわれるので、研磨による膜厚分布バラツキが発生し、超薄膜の均一形成が困難となる。同様の理由によりＳＯＩ層の研磨を必要とする方法では全て、超薄膜の直接形成は困難となる。

【0013】又、ＳＯＩ膜の平滑化のために前述の水素アニールを使うと、ピンホールが発生する事がある。貼り合せ界面に存在する。計測器では測定できないほど微小（９０ｎｍ以下）な異物や、ウエハ自体の表面凹凸により、超薄膜の貼り合わせ界面側の微小領域に応力がかかる。この応力の存在下で、水素アニール処理を行なうと、応力発生部位にピンホールが発生してしまうことがあるのである。一方、トランジスタ等の半導体デバイスの設計の際に、要求されるＳＯＩ膜厚が、ＳＯＩウエハーとして供給できる最小膜厚よりも更に薄い場合、或いは設計の変更に伴い異なる膜厚のＳＯＩウェハーが必要になる場合には、ウェハー供給側が十分に対応できない。そのような場合、半導体デバイスの製造者は、設計膜厚よりも厚いＳＯＩ層をもつＳＯＩウェハーを予め入手しておき、その表面を一旦熱酸化した後、酸化した部分をエッチングで除去するという犠牲酸化を行って、所望の膜厚のＳＯＩ層を得なければならない。

【0014】しかしながら、犠牲酸化を行うと、ＳＯＩ膜中に実存する結晶欠陥に対する増速酸化がなされたり、異物の付着した領域の周辺で酸化が阻害されたりするため、結果としてＳＯＩ層の表面の表面荒れを引き起こすことになる。これは半導体デバイスの酸化膜耐圧を劣化させる原因となる。

【0015】

【課題を解決するための手段】本発明の目的は、シリコン薄膜の品質を劣化させることなく、その膜厚を所望の値に減少させることができるシリコン薄膜の膜厚制御方法、シリコン薄膜の製造方法及び、ＳＯＩ基板の製造方法を提供することにある。

【0016】本発明は、絶縁性表面上に設けられたシリコン薄膜を製造するためのシリコン薄膜の製造方法において、前記絶縁性表面上に設けられたシリコン薄膜をウ

ェット洗浄することにより、１００ｎｍ以下の膜厚になるまで該シリコン薄膜の膜厚を減少させる工程を含むことを特徴とする。また、本発明に係るシリコン薄膜の製造方法は、前記ウェット洗浄する前の前記シリコン薄膜の第１の厚さは、１００ｎｍより大きく、該第１の厚さを有する該シリコン薄膜を水素を含む還元性雰囲気中で熱処理した後、該第１の厚さよりも薄い第２の厚さになるまで該ウェット洗浄を行うことを特徴とする。たとえば、前記第２の厚さが１００ｎｍ以下あるいは５０ｎｍ以下である。

【００１７】本発明に係るＳＯＩ基板の作成方法は、絶縁性表面上に１００ｎｍより大きい第１の厚さのシリコン薄膜を有する基体を用意する工程、該基体を水素を含む還元性雰囲気中で熱処理する熱処理工程、及び該熱処理工程の後、該基体をウェット洗浄し、該シリコン薄膜を該第１の厚さより薄い第２の厚さの膜厚にする工程を含むことを特徴とする。

【００１８】前記基体が、多孔質層上にシリコン薄膜を有する第１の基板と第２の基板を絶縁層を介して貼り合わせて複合部材を形成した後、該複合部材を多孔質層で分離する工程を含み形成されたり、イオン注入層上にシリコン薄膜を有する第１の基板と第２の基板を絶縁層を介して貼り合わせて複合部材を形成した後、該複合部材を該イオン注入層で分離する工程を含み形成される。

【００１９】本発明によれば、従来の犠牲酸化を行う際に生じた結晶欠陥部の増速酸化や、異物の影響などによる表面荒れ、表面荒れに伴う酸化膜耐圧の劣化などを回避できる。また、熱酸化工程及び熱酸化膜のエッチング工程を省くことができる。

【００２０】

【発明の実施の形態】本発明においては、まず図１に示すようにＳＯＩ基板５０を用意し、そのＳＯＩ基板の絶縁層４上にあるシリコン薄膜（ＳＯＩ層）３を熱酸化することなく、ウェット洗浄する。このウェット洗浄によりＳＯＩ層の膜厚を減少せしめて所望の膜厚を得る。なお、１０はシリコンなどの基体である。

【００２１】本発明に用いられるＳＯＩ層としては、上述したＳＩＭＯＸ法、貼り合せ法により作製されたＳＯＩウエハのＳＯＩ層が好ましい。そして、エピタキシャル成長或いは水素アニールにより形成されたシリコン薄膜を用いて形成したＳＯＩ層、又はＦＺ（フローティングゾーン）法により形成されたシリコン基板を用いて作製されたＳＯＩ層は、一般的なＣＺ（チョクラルスキー）法により形成されたシリコンウエハより、酸素含有率が低いために、より好ましいものである。また、ＭＣＺウエハも好ましいものである。こうして得られたＳＯＩ層は、その中に酸化シリコン等の析出物がなく、均質なシリコン薄膜となっている。シリコン薄膜を指示する基板としては、絶縁膜が表面に形成された半導体又は導電岱の基板或いは絶縁体基板である。

【００２２】シリコン以外の物質がシリコン薄膜中に析出していると、その部分での均一な酸化や均一なエッチングが阻害されるからである。

【００２３】ＣＺ（チョクラルスキー）法にて得られるシリコンウェハーをＳＯＩ層にした場合には、酸素の析出によりシリコン中に欠陥が発生したり、表面の荒れが生じてしまう。ＣＺシリコンウエハ中に多く含まれる酸素は、水素によって還元され、その濃度が低くなって析出が抑えられる。よって、水素アニールされたＳＯＩ層としては、水素アニールを施すことなくＳＯＩ層を形成した後、そのＳＯＩ層に水素アニールを施したものであってもよいし、水素アニールしたシリコンウエハを用いてＳＯＩ層を形成したものであってもよい。

【００２４】本発明により膜厚を減じる前のＳＯＩ層の膜厚は１００ｎｍより大きく、最終的に得られるＳＯＩ層の膜厚は、１００ｎｍ以下という極めて薄い膜である。

【００２５】本発明に用いられる洗浄液としては、所謂ＲＣＡ洗浄で用いられるＳＣ１洗浄液が好適である。ＳＣ１洗浄液は、NH_4OH、H_2O_2 、H_2Oの混合液からなる。その混合比の代表例は標準的なアンモニア水、過酸化水素水、水が容量比で１：５：５、１：１０：１０、０．０５：１：５、０．０５：１：１０などまちまちであり、２：５：５～０．０１：１：５であっても良い。なお、ここにいうアンモニア水、過酸化水素水の濃度は、例えばそれぞれ２９％、３１％のものを用いることができる。

【００２６】本発明の洗浄時の液温は高い方が洗浄、エッチングの能力がともに高い、概して６０℃以上の温度、より好ましくは６０℃～９５℃である。

【００２７】この他に有機アルカリ系溶液でも、概してシリコンエッチングの能力がある。例えばＴＭＡＨ（テトラ・メチル・アンモニウム・ハイドロオキサイド）などは、半導体デバイス製造ラインのホトリソグラフィー工程で、ホトレジストの現像液としても広く使われている材料であるが、本発明の洗浄液としても有効である。

【００２８】シリコンのエッチャントとしてはフッ酸、硝酸の混合液などもありえるが、この系では結晶欠陥を選択的にエッチングするなど、ＳＯＩ表面を荒らす場合があるので使用時には注意が必要である。

【００２９】

【実施例】（第１実施例）図２及び図３を用いて本発明の一実施例について説明する。

【００３０】図２は多孔質層とエピタキシャル成長層を利用したＳＯＩウェハーの製造工程を説明するための模式図である。図３は陽極化成装置を示す模式図である。図３において、１０２は陽極化成槽、１０３は基板ホルダー、１０５は基板ホルダーの開口部、１０４は減圧吸着パッド、１０６は陽極化成用の電解液、１０７，１０８は陽極化成用の電流を供給するための電極端子、１０

9は減圧ラインである。

【0031】まず、シリコン基板1として、P型で比抵抗が0.015Ωcmの8インチデバイスウェハーを用意した。

【0032】このデバイスウェハー101を、陽極化成槽102の中に置かれたホルダー103の吸着パッド104にデバイスウェハー101の表面を接触させ、パッド104の吸着溝（不図示）につながっている減圧ライン109によって減圧吸着して固定した。

【0033】この状態で槽102に、電解液として、フッ化水素酸：エタノール＝2：1の混合液を満たした。

【0034】そして化成槽の両端に設けられた白金製のマイナス電極107、とプラス電極108との間に、まず、第1の電流値（2.5アンペア）で5分間通電し、続いて第2の電流値7.2アンペアに変更して1分間通電した。その結果、デバイスウェハー1の表面から5μmの深さまでが第1の多孔質シリコン層21となり、更に2μm深さまでが第1の多孔質シリコン層より高多孔度で且つ薄い第2の多孔質シリコン層22となり、こうして互いに多孔度の異なる複数多孔質体からなる多孔質層2が形成された。

【0035】次に、400℃にて熱酸化を行い第1及び第2の多孔質層2の孔壁面に薄い酸化膜を形成した。そして、希フッ化水素酸にて洗浄を行った後、CVD装置にデバイスウエハを配して水素ガスを流しながら温度を上げて、多孔質層2を水素ベークした。続いて、水素キャリアガスとともにジクロロシラン（SiH_2Cl_2）を流して、1050℃で、第1の多孔質層2の表面に、エピタキシャル成長を行ない、150nmの非多孔質の単結晶シリコン膜3（SOI層）を形成した（図2C）。

【0036】次いで、単結晶シリコン膜3の表面を熱酸化して、100nmの酸化シリコン層4を形成した（図2D）。この酸化シリコン層の形成は省略することもできる。

【0037】別に用意しておいたハンドルウェハー10を洗浄した後に、デバイスウエハの酸化シリコン層に洗浄な雰囲気中で室温で貼り合わせた（図2F）。なお、デバイスウエハ1のSOI層3（あるいは、その上に形成された酸化シリコン層4）とハンドルウエハ10とを貼り合わせる際には、デバイスウエハは、シリコン基板であったり、シリコン基板上に絶縁膜を有していたり、光透過性基板や絶縁性のフィルムであってもよい。

【0038】この貼り合わせたウェハー（多層構造体）を1100℃の窒素雰囲気中で2時間熱処理した後に、ウエハの側面から貼り合わせ界面向けてくさびを挿入し、2つの多孔質シリコン層21と22の凡そ界面において分離した（図2G）。

【0039】このようにしてハンドルウェハー10に、酸化シリコン層4、単結晶シリコン膜3が移設されたウエハが得られた。単結晶シリコン膜3の表面上には多孔質シリコン層21が残留していた。（図2G）。

【0040】次にこのウェハーをフッ化水素酸：過酸化水素水：水＝1：20：50の混合液に浸し、超音波を印加しながら約90分間の時間をかけて、多孔質シリコン層21を選択エッチングにより除去した。

【0041】このウェハーの表面を平滑にするために、1100℃の水素アニールを1時間施し、シリコン層100nm、埋め込み酸化膜100nmのSOIウェハーを得た（図2H）。

【0042】続いて得られたSOIウェハーの単結晶シリコン膜（SOI層）3の厚みをより薄く制御するために、このSOIウェハーを、85℃に加熱された。組成が容量比でアンモニア水：過酸化水素水：水＝0.05：1：10のSC1溶液に浸し洗浄した。この洗浄工程によるエッチンググレートは、0.5nm／分であったので、洗浄を140分間継続し、SOI層103を70nmエッチング除去した。

【0043】なお、アンモニア水の濃度は29%、過酸化水素水31%である。

【0044】結果として、SOI層の厚さが30nm、埋め込み酸化シリコン層の厚さが100nmの超薄膜SOIウェハーが得られた。

【0045】このSOIウェハーの表面を観察してみると、水素アニール処理をした直後と殆ど変ることなく極めて平滑で、且つ均一な表面であった。

【0046】〈比較実験①〉犠牲酸化により薄膜化する場合と本発明のように洗浄して薄くする場合との比較実験を行った。

【0047】具体的には、上述のように前記アンモニア水／過酸化水素水／水の混合液で洗浄して膜厚を70nmエッチングしたSOIウェハー（試料A）とは別に、熱酸化によりSOI層を約150nm酸化した後、その酸化膜を希フッ酸にてエッチングし、結果としてSOI膜厚を約70nm減らしたSOIウェハー（試料B）を用意した。

【0048】SOI層の表面性の比較を行う為、両者を濃フッ酸に15分間浸漬した後、その表面を顕微鏡で観察することを行った。

【0049】その結果、試料Bは、直径約50μmのボイド（SOI層の欠陥、或は貫通孔を通ってフッ酸が埋め込み酸化膜層に達し、次いで埋め込み酸化膜がフッ酸によりエッチングされたために形成されるSOI膜下の空隙：通称HFボイド）が約5個／cm^2の密度で観察された。一方、試料Aは、所謂HFボイドの密度は0.05個／cm^2にとどまった。

【0050】試料B即ち、熱酸化したウェハーのHFボイド密度が高かったのは、酸化工程においてSOI中に含まれる結晶欠陥が増速的に酸化され、HF溶液に浸した際にその部分がエッチングされて極めて薄くなり、SOI部分に孔が空いて、HFボイドが形成され易くなっ

たものと推察される。

【0051】〈比較実験②〉上記『多孔質シリコンのエッチング（1）』、『水素アニール（2）』、『洗浄による膜厚減らし（3）』の順番を決めるにあたっては次のような実験を行い決定した。上記工程を（1）→（3）→（2）で行ってみたところ（これはSOI膜を薄くしてから水素アニールによる平坦化を行うことになる）これを行った結果、水素アニール後のウェハー表面を顕微鏡観察したところ四角形のピットと思われるものが多数観察された。これは30nmという極めて薄いシリコン膜にアニールの熱ストレスが影響を及ぼし、結晶欠陥部分若しくは局所的に薄くなっていた部分により大きな応力が集中し、アニール雰囲気下で膜に孔が開いたためと考えらえる。孔が開くとシリコンとシリコン酸化膜の境界が露出するが、それが水素雰囲気中で$Si+SiO_2 \rightarrow 2SiO$という反応が起こり、シリコン及びシリコン酸化膜がガス化して孔を拡大するのである。この理由により、薄膜SOI層の作製には、SOI膜厚が比較的厚みを持った状態でアニールする必要があることを見い出し、（1）→（2）→（3）という順番で薄膜化行う本発明を成すに至った。

【0052】SOI層を水素アニールずる場合は、その時点での膜厚が70nm以上、より好ましくは100nm以上であることが好ましい。但し、埋め込み酸化膜層が十分に厚い場合は、この限りではない。例えば、埋め込み酸化膜が500nm程度の厚みを有する場合には、水素アニール前のSOI層の膜厚は、50nm程度でもよい。埋め込み酸化膜の厚みが100nm程度のときは、SOI層の膜厚は70nm以上であるのがよい。

【0053】（多孔質層の形成）ウェハ表面への多孔質層の形成は陽極化成により行うことができ、電流密度や化成溶液の種類あるいはその濃度を変えて、互いに多孔度の異なる2層、あるいは3層以上の複数の多孔質層を形成することも出来る。

【0054】とりわけ、多孔質層の構成は外側表面から第1の多孔度を有する第1の多孔質層、該第1の多孔度より大きい第2の多孔度を有する第2の多孔質層をこの順に有することが好ましい。当該構成により第1の多孔質層上に、欠陥等の少ない非多孔質層（たとえば、非多孔質単結晶シリコン層）が形成できると共に多孔質層の所望の位置での分離が可能となる。

【0055】第1の多孔度としては、10%～30%、より好ましくは15%～25%であることが望ましい。また、第2の多孔度としては、35%～70%、より好ましくは40%～60%であることが望ましい。

【0056】陽極化成用の化成液としては、フッ化水素を含む溶液、フッ化水素とエタノールを含む溶液やフッ化水素とイソプロピルアルコールを含む溶液などを用いることができる。

【0057】（非多孔質層の形成）ここで多孔質層上に非多孔質層を形成するに先立って、下記の（イ）～（ニ）の工程の少なくとも1つを付加することもできる。好ましくは、（イ）→（ロ）、より好ましくは（イ）→（ロ）→（ハ）、あるいは（イ）→（ロ）→（ニ）、更に好ましくは（イ）→（ロ）→（ハ）→（ニ）と一連の工程を行うことがよい。

【0058】（イ）孔壁への保護膜形成工程
多孔質層の孔壁に酸化膜や窒化膜などの保護膜を設け、熱処理による孔の粗大化を防いでもよい。例えば、酸化性雰囲気で熱処理（200℃～700℃、好ましくは300～500℃）を行う。その際多孔質層の表面に形成された酸化膜等を除去（例えばHFを含む溶液に表面をさらす。）してもよい。

【0059】（ロ）水素ベーキング工程
多孔質層上への非多孔質層の形成に先だって、水素を含む還元性雰囲気中800℃～1200℃で熱処理することも好ましいものである。当該熱処理により多孔質層表面の孔をある程度封止することが出来ると共に、多孔質層表面に自然酸化膜が存在する場合にはそれを除去することも可能である。

【0060】（ハ）微量原料供給工程
多孔質層上へ非多孔質層を成長する場合、成長初期段階において該非多孔質層の原料物質を微小量供給し、低速度で成長させることが好ましい。かかる成長により多孔質層表面の原始のマイグレーションが促進され孔表面を封止することができる。

【0061】具体的には、成長速度が20nm／min.以下、好ましくは10nm／min.以下、より好ましくは2nm／min.以下の成長速度となるように供給原料を調節する。

【0062】（ニ）高温ベーキング工程
前述の水素ベーキング工程及び／又は、微量原料供給工程における処理温度よりも高い温度で、かつ水素を含む還元性雰囲気中で熱処理することにより、多孔質層表面のより一層の封止、平滑化が可能となる。

【0063】多孔質層上への非多孔質層の形成は、ホモエピタキシャル成長あるいはヘテロエピタキシャル成長が可能である。非多孔質層としては、Si、Ge、SiGe、SiC、C、GaAs、GaN、AlGaAs、InGaAs、InP、InAs等が可能である。

【0064】（非多孔質層の移設方法）多孔質層上へ形成された非多孔質層を支持基板あるいはフィルム等へ移設する方法としては、貼り合わせ工程より得られる多層構造体から研削、研磨、エッチングあるいはこれらの組み合わせにより不要な非多孔質部を除去し、その後表出した多孔質層をエッチング（エッチャント：$HF+H_2O_2$ or HF＋アルコール、$HF+H_2O_2$＋アルコール）等により除去したり、該多層構造体を多孔質層で分離する方法がある。

【0065】分離は、該多層構造体に引張り力、圧縮

力、せん断力等を加えたり、該多層構造体側面に流体を吹きつけることにより行える。

【００６６】使用する流体としては、水、アルコールなどの有機溶媒やフッ酸、硝酸などの酸、あるいは水酸化カリウムなどのアルカリその他分離領域を選択的にエッチングする作用のある液体なども使用可能である。低温冷却流体、超冷却液体を用いることもできる。更に、流体として空気、窒素ガス、炭酸ガス、希ガスなどの気体を用いても良い。

【００６７】支持基板上へ移設された非多孔質層上に多孔質層が残留する場合には、エッチングや研磨により除去することが出来る。水素雰囲気中での熱処理により表面平滑化を図ることも可能である。

【００６８】こうして得られるＳＯＩウェハーを本発明による方法を用いて薄膜化する。

【００６９】（第２実施例）図４を参照して本発明の別の実施例によるシリコン薄膜の製造方法について説明する。

【００７０】まず基板として、Ｐ型で比抵抗が１０Ωｃｍの８インチのＣＺシリコンウェハー１を用意した（図４Ａ）。

【００７１】このウェハー表面にトリクロロシラン（$SiHCl_3$）を用いたＣＶＤによるホモエピタキシャル成長を行い、１０μｍのエピタキシャル層５を形成した（図４Ｂ）。

【００７２】続いてこのウェハー表面にドーズ量2×10^{18}／cm^2、加速エネルギー１８０ＫｅＶで酸素イオン６を打ち込み、エピタキシャル層５の膜中に酸素イオンを高濃度で含む層７を形成した（図４Ｃ）。酸素イオンとしては例えば、O^+である。

【００７３】なお、打ち込むに際して、エピタキシャル層５表面上に酸化膜などの絶縁膜を形成しておいてもよい。

【００７４】次に、このウェハーをアルゴン雰囲気中に置いて、１３５０℃で６時間の熱処理を施し、高濃度の酸素イオン含有層７を酸化シリコン層４に変化させた。こうして、エピタキシャル成長したシリコンから形成されたＳＯＩ層３の厚さは１９０ｎｍとなり、埋め込み酸化シリコン層４の厚さは３８０ｎｍとなった。

【００７５】このウェハーを第１の実施例と同様な組成のＳＣ１溶液に１８０分間浸して洗浄し、ＳＯＩ層３を１００ｎｍに薄膜化した。このＳＯＩ層の膜厚均一性は高く、且つその表面も極めて平滑なものであった。なお、埋込み酸化膜の厚膜化のためにいわゆるＩＴＯＸ法を用いてもよい。

【００７６】（第３実施例）図５を参照して本発明の別の実施例によるシリコン薄膜の製造方法について説明する。

【００７７】まず基板として、Ｐ型で比抵抗が１００Ωｃｍの６インチのＦＺシリコンウェハー１を用意した（図５Ａ）。

【００７８】続いて、このウェハー表面にドーズ量2×10^{18}／cm^2、加速エネルギー１８０ＫｅＶで酸素イオン６を打ち込み、ＦＺウェハーの表面より下の部分に酸素イオンを高濃度で含む層７を形成した（図５Ｂ）。

【００７９】第２実施例と同じ条件でアルゴン雰囲気中で熱処理を行い、ＳＯＩ層３の厚さが１９０ｎｍ、埋め込み酸化シリコン層４の厚さが３８０ｎｍのＳＯＩウェハーが得られた。

【００８０】続いて、ＨＦ濃度５ｗｔ％のフッ化水素酸に１分間、ＳＯＩウェハーを浸して、表面の自然酸化膜を完全に除去し、十分に純水リンスをした。

【００８１】そして、現像液として市販されているＴＭＡＨ濃度が２．３５ｗｔ％のＴＭＡＨ水溶液に、上記ＳＯＩウェハーを浸して、ＳＯＩ層３を、室温で２０分間、洗浄し、ＳＯＩ層３の表層を約１４０ｎｍ除去した。この水溶液によるシリコンのエッチング速度は、２５℃液温で約７ｎｍ／分であった。

【００８２】続いて、第１実施例で用いたものと同じＳＣ１溶液を用いてＳＯＩウェハーを５分間洗浄した。

【００８３】これにより第２実施例よりも短時間で、ＳＯＩ層を元の１９０ｎｍから、５０ｎｍに薄膜化することができた。

【００８４】（第４実施例）図６を参照して本発明の別の実施例によるシリコン薄膜の製造方法について説明する。

【００８５】まず基板として、Ｐ型で比抵抗が１０Ωｃｍの８インチＣＺウェハー１を用意した。

【００８６】このウェハーを水素雰囲気中に置いて、１２００℃で、６時間の熱処理を施し、ウェハー表面近傍の酸素析出物を還元し、酸素濃度を低減させた低酸素濃度層８を形成した（図６Ｂ）。

【００８７】この後は、第３実施例と同様に、酸素イオン６を打ち込んで、熱処理し（図６Ｃ）、埋め込み酸化シリコン層４を形成し（図６Ｄ）、その後エッチングと洗浄を連続に行い、第３実施例と同じ膜厚構成のＳＯＩウェハーを得た。

【００８８】（第５実施例）図７を用いて本発明の第６実施例について説明する。

【００８９】まずデバイスウェハーである８インチｐ型１０～２０Ωｃｍのシリコンウェハー７１を用意した（図７Ａ）。

【００９０】次いで７１の表面に通常のエピタキシャル法により、５μｍのシリコン層７２を成長させた（図７Ｂ）。なお、このエピタキシャル成長工程は省略することもできる。

【００９１】そして、このエピタキシャルシリコン層７２の表面を熱酸化し、４００ｎｍのシリコン酸化膜層７３を形成した（図７Ｃ）。なお、この酸化膜層形成工程は省略することもできる。

【００９２】次にイオン注入装置を用いて、シリコン酸化膜層７３の表面から水素イオンを注入した（図７Ｄ）。このときの注入エネルギーとドーズ量は、夫々１００ｋｅＶ、2×10^{15}／cm^2とした。この結果水素イオンは基板表面から約８００ｎｍの深さまで達し、イオン注入層７５を形成した。このイオン注入層には歪応力がかかっていると考えられる。なお、該イオン注入層は、シリコンウエハ７１内に形成しても、又、シリコン層７２とシリコンウエハ７１の界面付近に形成してもよい。

【００９３】次にもう１枚の支持ウェハーである８インチｐ型１０～２０Ωｃｍのシリコンウェハー７を用意し、この支持ウェハー７の表面とデバイスウェハー７１の表面（シリコン酸化膜層７３表面）を互いに洗浄した後に貼り合わせた（図７Ｅ）。ここで貼り合わせる前に貼り合わせ強度を高めるために、夫々のウェハーをプラズマ発生装置（不図示）に置き、窒素イオンを表面に曝す操作を行った。この操作によって貼り合わせ強度は、単に洗浄して貼り合わせるのみの場合に比べて、室温において約５倍の貼り合わせ強度が得られた。

【００９４】貼り合わせた基板に３００℃、１時間の熱処理を施して貼り合わせ強度を更に強固なものとした後、貼り合わせ界面付近に、エアジェットノズル７７を近付け、６ｋｇ／cm^2の圧力で圧搾空気７８を吹き付けた。その結果デバイスウェハー７１側のイオン注入層７５の層内で分離が起こり、イオン注入層７５を境にデバイスウェハー７１側と支持ウェハー７６側が完全に分離した（図７Ｆ）。尚この際に用いたエアジェットノズル７７の先端形状は、断面が０．１ｍｍ×６ｍｍの矩形をなしており、空気を吹き付ける際にはノズルの先端を、基板貼り合わせ界面から１ｍｍの位置に近付けて行った。

【００９５】この結果、支持ウェハー７６の上に４００ｎｍのシリコン酸化膜層７３、その上に約３５０ｎｍのエピタキシャルシリコン層７２、その上に約５０ｎｍのイオン注入層７５を有するＳＯＩ構造が得られた（図７Ｇ）。

【００９６】続いて得られたＳＯＩウェハーに１０５０℃、３時間の水素アニール処理を施し、イオン注入層７５のひずみを除去すると同時に分離によって荒れていた表面を極めて平滑な状態に改質せしめた。

【００９７】最後に平滑になったシリコンエピタキシャル層（ＳＯＩ層）７２を、第２実施例と同様な現像液に浸して洗浄膜減らしを行った。この際の現像液は２．３５ｗｔ％のＴＭＡＨ溶液を８０℃に加熱したものを用い、この液中に４分間浸すことによって３２０ｎｍ、更に第１実施例で用いたＳＣ－１液に２０分間浸すことによって１０ｎｍ、合計３３０ｎｍの膜減らし洗浄を行い、結果として７０ｎｍのシリコンエピタキシャル層（ＳＯＩ層）２と、４００ｎｍのシリコン酸化膜層（埋め込み酸化膜層）３を有するＳＯＩウェハーが完成した。

【００９８】なお、分離領域形成のためのイオン注入種は、水素やＨｅ等の希ガスである。また、イオン注入法は、ビーム状に注入していったり、プラズマ浸漬イオン注入法（ＰＩＩＩ　ｔｅｃｈｎｉｑｕｅ）を用いることができる。吹きつける流体としては、空気の他に窒素やアルゴン等の気体であってもよい。これらのことに関しては、国際公開公報９８／５２２１６に詳しい。

【００９９】（半導体装置の製造方法）図８を参照して、以上説明した本発明の各実施形態による半導体基体を用いた半導体装置及びその製造方法について述べる。

【０１００】半導体基体として上述の実施例１～７等に記載の本発明を用いて形成されたＳＯＩウェハ５０を用意する。

【０１０１】基材５１上の埋め込み絶縁膜５２上にある非多孔質半導体からなるＳＯＩ層を島状にパターニングしたり、ＬＯＣＯＳ酸化を施して、トランジスタを形成すべき領域のＳＯＩ層のパターン５３を形成する。図では、絶縁体などの素子分離領域５４を用いた場合の様子を例にあげて示してる。

【０１０２】ＳＯＩ層５３の表面にゲート絶縁膜５６を形成する。ゲート絶縁膜５６としては、酸化シリコン、窒化シリコン、酸化窒化シリコン、酸化アルミニウム、酸化タンタル、酸化ハフニウム、酸化チタン、酸化スタンジウム、酸化イットリウム、酸化ガドリニウム、酸化ランタン、酸化ジルコニウム及びこれらの混合物ガラスなどが用いられる。このゲート絶縁膜５６は、ＳＯＩ層５３の表面を酸化したり、又はＣＶＤやＰＶＤによりＳＯＩ層５３の表面に堆積することにより形成できる。

【０１０３】ゲート絶縁膜５６の上にゲート電極５５を形成する。ゲート電極５５としては、Ｐ型又はN型不純物がドープされた多結晶シリコンや、タングステン、モリブデン、チタン、タンタル、アルミニウム、銅などの金属（これらを少なくとも一種含む合金を含む）や、モリブデンシリサイド、タングステンシリサイド、コバルトシリサイドなどの金属珪化物や、チタンナイトライド、タングステンナイトライド、タンタルナイトライドなどの金属窒化物が用いられる。これらの材料の層はポリサイドゲートのように複数種類積層されて用いられても良い。ここでは、サリサイド（セルフアラインシリサイド）と呼ばれるプロセスでゲート電極を形成する場合について述べるが、ダマシンゲートプロセスと呼ばれる方法で形成してもよい。

【０１０４】こうして、図８（ａ）に示すような構造体が得られる。

【０１０５】ゲート電極５５のパターンを形成した後、リン、砒素、アンチモンなどのN型不純物又はボロンなどのＰ型不純物をＳＯＩ層５３に導入して、ゲート電極５５の側面に整合した比較的低濃度のソース、ドレイン

領域５８を形成する。不純物はイオン打ち込みと熱処理などにより導入できる。

【０１０６】ゲート電極５５を覆うように絶縁膜を形成した後、エッチバックしてゲート電極５５の側面にサイドウエール５９を形成する。

【０１０７】再び同じ導電型の不純物を導入し、サイドウオール５９に整合した比較的高濃度のソース・ドレイン領域５７を形成する。

【０１０８】こうして、図８（ｂ）に示す構造体が得られる。

【０１０９】ゲート電極上面とソース・ドレイン領域の上面を露出させて、そこに金属半導体化合物の層６０を形成する。金属半導体化合物としては、金属珪化物が好ましく、具体的にはニッケルシリサイド、チタンシリサイド、コバルトシリサイド、モリブデンシリサイド、タングステンシリサイドなどが用いられる。これらの珪化物は、ゲート電極５５の上面とソース・ドレイン領域５７の上面を覆うように金属を堆積させて、熱処理を施してソース・ドレイン領域５７のシリコンと反応させた後、金属の未反応部分を硫酸などのエッチャントで除去することにより形成できる。必要に応じて更に、金属半導体化合物の層６０の表面を窒化してもよい。

【０１１０】こうして、図８（ｃ）に示す構造体が得られる。

【０１１１】シリサイド化したゲート電極上面、ソース・ドレイン領域上面を覆うように絶縁膜６１を形成する。この絶縁膜６１としては、リン及び／又はボロンを含む酸化シリコンなどが好ましく用いられる。

【０１１２】必要に応じて、エッチバックやＣＭＰにより絶縁膜６１の上面を平坦化して、絶縁膜６１にコンタクトホールを形成する。ＫｒＦエキシマレーザ、ＡｒＦエキシマレーザ、F_2エキシマレーザ、電子ビーム、Ｘ線を光源とするフォトリソグラフィーを用いれば、０．２５ミクロンより小さい長さの一辺をもつ矩形のコンタクトホール、または０．２５ミクロンより小さい長さの一辺をもつ直径をもつ円形のコンタクトホールが形成できる。

【０１１３】コンタクトホール内に導電体プラグを形成する。コンタクトホール内の導電体プラグの形成方法としては、バリアメタル６２となる高融点金属膜、金属半導体化合物又は高融点金属窒化物からなる少なくとも一つの層を形成した後、タングステン、タングステン合金やアルミニウム、アルミニウム合金、銅、銅合金などの導電材料６３を、ＣＶＤ、ＰＶＤ、メッキ法を用いて堆積させ、必要に応じて絶縁膜上面より上にある導電材料をエッチバックやＣＭＰにより除去してもよい。

【０１１４】或いは必要に応じてコンタクトホールから露出したソース・ドレイン領域５７のシリサイド層６０の表面を窒化した後、コンタクトホール内に導電体を充填してもよい。

【０１１５】こうして、図８（ｄ）に示したような構造体（ＭＯＳ型薄膜トランジスタ）が得られる。

【０１１６】こうして、本発明のＳＯＩウェハを利用して、トランジスタなどの半導体装置が製造できる。

【０１１７】このときに、ゲート電極に電圧を印加してゲート絶縁膜下に広がる空乏層が埋め込み絶縁膜の上面に届くようにＳＯＩ層の厚さ及び不純物濃度を定めれば、このトランジスタは完全空乏型トランジスタとして動作する。また、空乏層が埋め込み絶縁膜の上面に届かないようにＳＯＩ層の厚さ及び不純物濃度を定めれば、このトランジスタは部分空乏型トランジスタとして動作する。

【０１１８】本発明を用いた場合、ＳＯＩ層の薄膜化が可能であるので、完全空乏型トランジスタの形成が容易となる。

【０１１９】

【発明の効果】本発明によれば、従来の犠牲酸化を行う際に生じた結晶欠陥部の増速酸化や、異物の影響などによる表面荒れ、表面荒れに伴う酸化膜耐圧の劣化などを回避できる。また、熱酸化工程及び熱酸化膜のエッチング工程を省くことができる。こうして、今まで直接作成するのが困難であった超薄型（１００ｎｍ以下）のＳＯＩウェハーを、表面を荒らすことなく均一な膜厚に形成することが可能になる。

【図面の簡単な説明】

【図１】本発明を説明するための模式図である。

【図２】本発明の一実施形態によるシリコン薄膜の製造方法を説明するための模式図である。

【図３】陽極化成装置を示す模式図である。

【図４】本発明の実施形態によるシリコン薄膜の製造方法を説明するための模式図である。

【図５】本発明の実施形態によるシリコン薄膜の製造方法を説明するための模式図である。

【図６】本発明の実施形態によるシリコン薄膜の製造方法を説明するための模式図である。

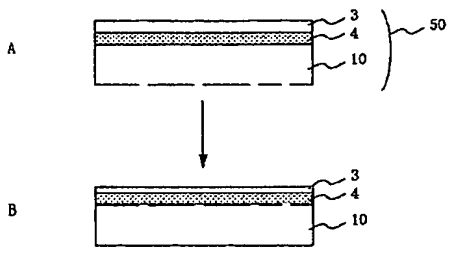
【図７】本発明の実施形態によるシリコン薄膜の製造方法を説明するための模式図である。

【図８】本発明により作製されたＳＯＩウェハを用いた半導体装置の製造方法についての模式図である。

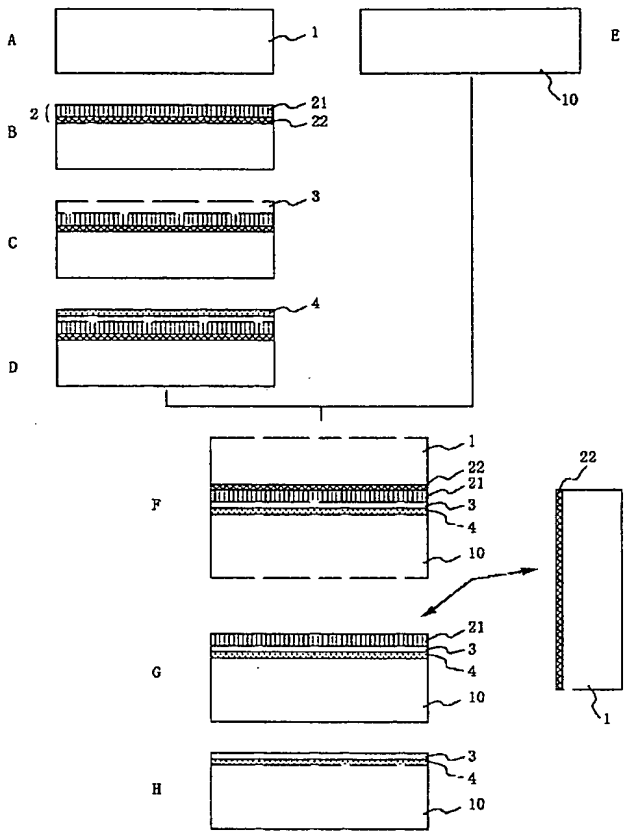
【符号の説明】

１　シリコン基板
２　分離層
３　シリコン薄膜
４　酸化シリコン層

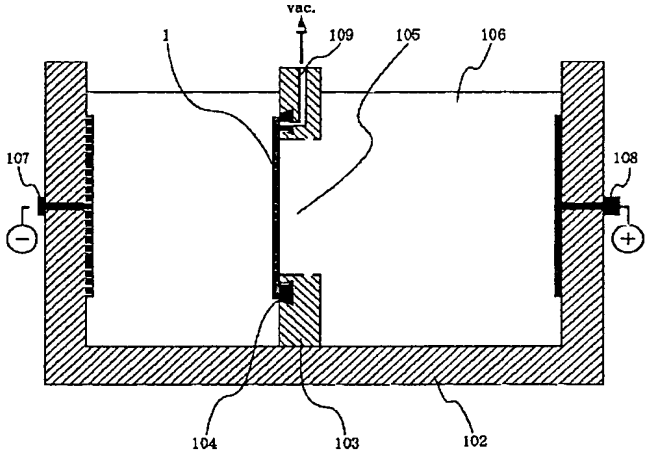
【図1】


A
B
3
4
10
50

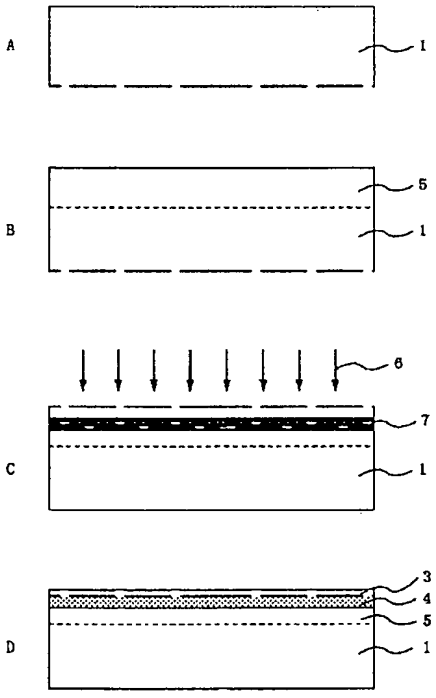
【図2】


A
B
C
D
E
F
G
H
1
2
21
22
3
4
10

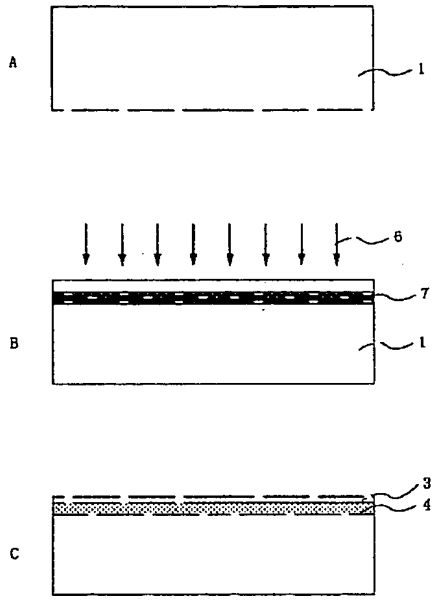
【図3】


vac.
1
109
105
106
107
108
104
103
102

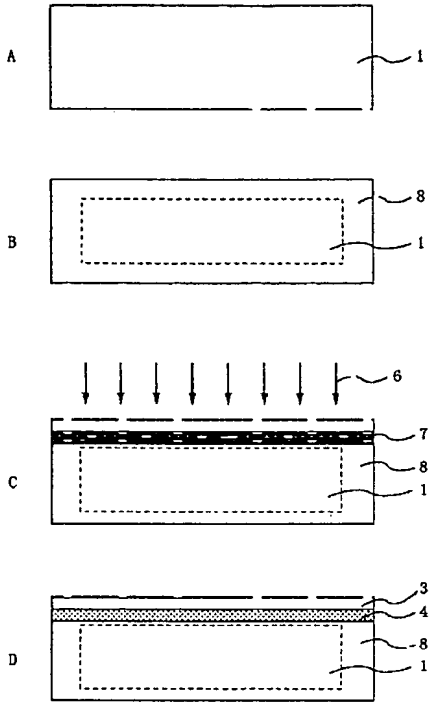
【図4】


A
B
C
D
1
5
6
7
3
4

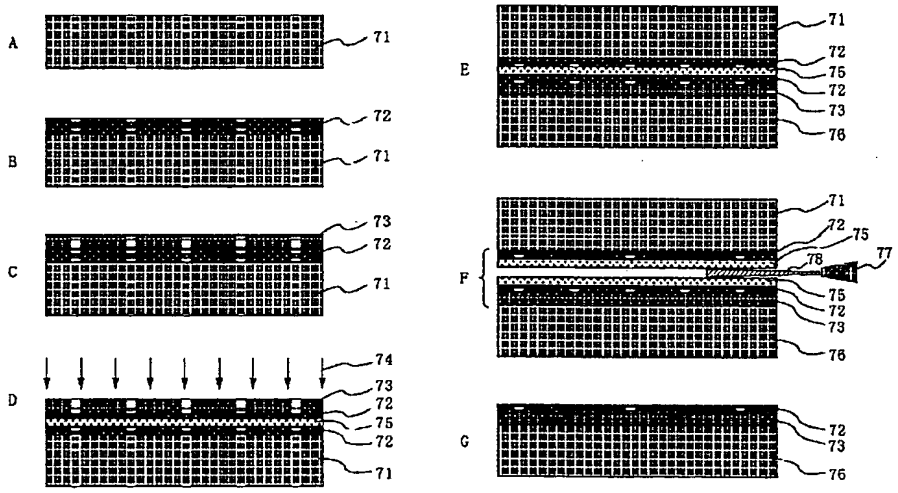
【図5】


A
1
6
7
B
1
3
4
C

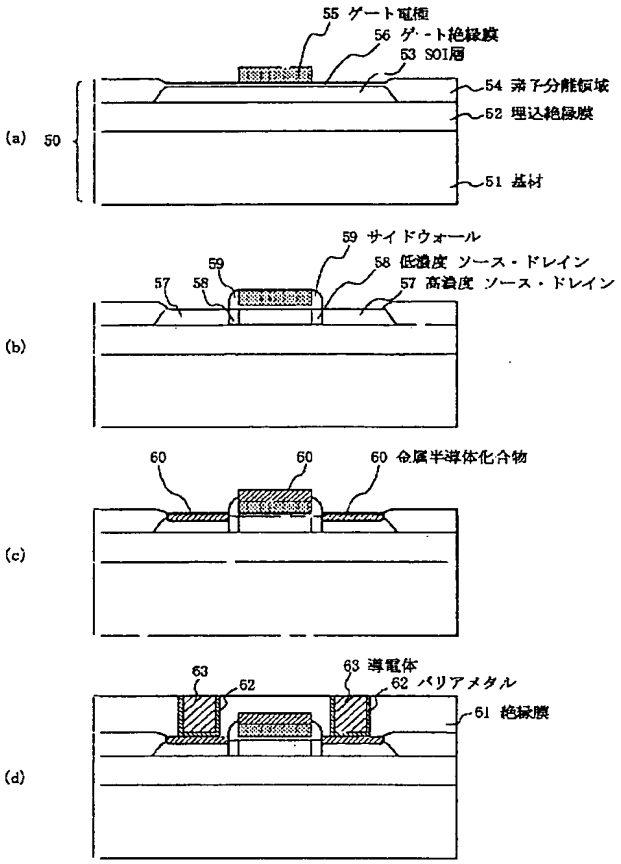
【図6】


A
1
8
B
1
6
7
8
C
1
3
4
8
D
1

【図7】


A
71
72
B
71
73
72
C
71
74
73
72
75
72
D
71
E
71
72
75
72
73
76
71
72
75
77
78
F
75
72
73
76
G
72
73
76

【図8】


55 ゲート電極
56 ゲート絶縁膜
53 SOI層
54 素子分離領域
52 埋込絶縁膜
(a) 50
51 基材
59 サイドウォール
59
58 低濃度 ソース・ドレイン
57 58
57 高濃度 ソース・ドレイン
(b)
60 60 60 金属半導体化合物
(c)
63 62
63 導電体
62 バリアメタル
61 絶縁膜
(d)